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Sub-micron PMOS transistor using electron beam lithography

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SUB-MICRON PMOS TRANSISTOR USING ELECTRON BEAM LITHOGRAPHY

by

Mark Klare

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Fabrication of a Sub-Micron PMOS Transistor Using E-Beam Lithography at The Rochester Institute of Technology

1. Abstract

The design, simulation, fabrication and testing of .75um PMOS transistors is studied in this work. The process uses Direct Write Electron Beam Lithography for all lithography steps. The process is matched for the tool set at The Rochester Institute of Technology and their accompanying process hurdles.

As of the beginning of this work, there had been no work done on obtaining a sub-micron transistor due to limitations in the optical lithography tools available at The Rochester Institute of Technology. A process flow that is robust, but as efficient as possible is used to obtain a working sub-micron PMOS transistor.

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2. Introduction

As general knowledge suggests, the move to smaller linewidth transistors will bring about great advancements in die size, speed, and cost of producing Semiconductor circuitry in the future. Because of this, there will always be people looking to ways of creating and fabricating smaller transistors.

This work will focus on designing, simulating, processing, and some minor analysis a .75um PMOS, poly gate transistor. The lithography will be done using an ETEC MEBES I direct write electron beam lithography tool. The basic theory of semiconductor MOSFETS is discussed along with analysis techniques used to characterize these transistors. Also, the direct write process and all processing steps needed to produce a sub-micron transistor is presented.

3. Historical Review

The history of sub-micron transistors at R.I.T. is very small. There has not been any concerted effort until now to create such a device. In the industrial world, however, there is a different story to tell. There has always been and will always be a need for smaller transistors. This will reduce cost, increase yield and increase the speed of most semiconductor chips. There has been some work of recent to create short channel transistors using Electron Beam Lithography. [1]

The benefit is a reduced linewidth during processing. The drawbacks are the thruput of wafers on direct write systems. This has been very slow in the past and does not seem to be able to keep up with stepper based lithography.

4. Theory

4.1. Basic Parameters

There are several basic equations that describe the characteristics of MOS semiconductor materials and help in describing how a simple PMOS transistor should operate. Using the parameters chosen for this devise, the following discussion will point to theoretical properties of such a transistor.

One of the basic parameters that needs to be known for MOS characterization is the work functions of both the bulk silicon and the gate material. The workfunction of a material is the voltage difference between the fermi level of intrinsic silicon and it's own fermi level. It is a calculated parameter that can be determined by substituting the dopant concentration of the concerned material into the following equation:

$$\Phi_{p-type} = \Phi_t * Ln\left(N_A / n_i\right) \qquad \text{Equation 1.}$$

$$\Phi_{n-type} = -\Phi_t * Ln\left(N_D / n_i\right) \qquad \text{Equation 2.}$$

where $\Phi_t = .0259V$.

The gate to bulk workfunction difference is the voltage difference between the two fermi levels as seen in the following equation:

$$\Phi MS = \Phi Gate - \Phi Bulk \qquad \text{Equation 3.}$$

The next parameter to look at is the mobility of the carriers in the bulk silicon μ_p. There has been much work done in determining the mobility of a substrate. Mobilities can be drawn from graphs in most basic semiconductor literature. [2]

Mobility is a very useful parameter when trying to characterize the current flow in the bulk of a silicon wafer. When dealing with a MOSFET, however, the electrical current is flowing at the silicon/oxide interface in an inversion layer created by the gate voltage. This is a totally different situation. Due to the small channel lengths in this transistor, and Drain voltages equivalent to gate voltages, the mobility will be different at each point along the transistor. To deal with this, an effective mobility (μ_{eff}) will be used to describe an overall mobility throughout the channel. The effective mobility used further in this paper will be:

$$u_{eff} = u_P * 0.6 \qquad \text{Equation 4.}$$

Another parameter that is used often in transistor characterization is Co, the oxide capacitance. This is solely a function of the gate oxide thickness. It is simply found by solving for the following equation:

$$C_O = \frac{K_O \varepsilon_O}{X_O} \qquad \text{Equation 5.}$$

where Ko is the dielectric constant for SiO2 and Eo is the permittivity of free space. With these basic parameters determined, we can now move on to some Capacitance-Voltage characterization.

4.2. Capacitance Voltage

One way of determining many important parameters of a MOS transistor is doing Capacitance/Voltage measurements on capacitors made under the same conditions as the transistors that are being analyzed. The following will give an introductory understanding of C-V measurement techniques and analysis.

As is well known, a PMOS devise is made up of four terminals, the Gate, Source, Drain and the Bulk Silicon. When making C-V measurements, the structure that is used is equivalent to a MOS transistor without the Source and Drain. Or in other words, a MOS capacitor.

A capacitor is made up of two conducting plates separated by an insulator. In this work, the two conducting plates are the P+ Poly gate and the N- well in bulk silicon. Running capacitance tests on metals is an easy excersize, but because of the characteristics of silicon devices, MOS C-V measurements take on a whole new angle. To get the most out of CV measurements on MOS devices, capacitance's must be looked at for high and low frequency effects, and in the three major regions of operation: accumulation, depletion and inversion.

Lets look at the MOS capacitor when the voltage applied leaves the bulk silicon in accumulation. When the bulk is in accumulation, an AC voltage can be reacted to by the majority carriers quite well. This leads to a straightforward analysis of the capacitance as follows:

$$C_{(acc)} \cong C_O = \frac{K_O \varepsilon_O A_G}{x_O} \qquad \text{Equation 6.}$$

where Ag is the area of the MOS capacitor.

In depletion, the capacitor is effectively made up of two capacitance's. The first is the oxide capacitance mentioned above and the second is the semiconductor capacitance made from the varying depletion region. Since the depletion width varies only as majority carriers are withdrawn from the depletion region, the charges on each side of the oxide can react to the ac signal. The semiconductor capacitance is as follows:

$$C_{(S)} = \frac{K_{Si}\varepsilon_O A_G}{W}. \qquad \text{Equation 7.}$$

Where W is the depletion width.

Putting Co and Cs in series gives the following equation:

$$C_{(Depl)} = \frac{C_O C_{GS}}{C_O + C_S} = \frac{C_O}{1 + \frac{W}{\frac{K_{Si} x_O}{K_O}}}. \qquad \text{Equation 8.}$$

When inversion sets in, there are two different reactions of the capacitor when a low frequency and a high frequency ac bias are applied. In inversion, there is a build-up of minority charges at the oxide/bulk surface. When a low frequency ac voltage is applied, the generation/recombination rate of the minority carriers is fast enough to respond. Therefore the capacitance is fixed back at Co, the oxide capacitance only When the frequency is increased to a certain point, the gen./recomb. cannot keep up, leaving the inversion charge constant around the dc voltage state. The charge difference is taken up by fluctuations in the depletion width. In inversion, the depletion width is fixed at Wt, therefore the inversion capacitance is:

$$C_{(Inv)} = \frac{C_O C_{GS}}{C_O + C_S} = \frac{C_O}{1 + \frac{W_T}{\frac{K_{Si} x_O}{K_O}}} .$$ Equation 9.

Once the C-V curve has been obtained, there are several parameters that can be extracted. The most important parameter will be the Flatband voltage Vfb. This is the voltage applied that gives zero band bending at the oxide/silicon interface. It is the dividing line between accumulation and depletion. To find Vfb, the Flat band capacitance, Cfb, must be found. This is a calculated parameter and is set by the device characteristics. Flat band capacitance is determined by taking two capacitance's in serial as in the case of C_{Depl}. In this instance, we need to take the oxide capacitance in series with the DeBye capacitance. To find the DeBye capacitance, the Debye length, Ld, must first be found and is defined as:

$$L_D = \left[\frac{K_{Si} \varepsilon_O}{2 q N_D} \frac{kT}{q} \right]^{1/2}$$ Equation 10.

The DeBye capacitance is:

$$C_{(D)} = \frac{K_{Si} \varepsilon_O A_G}{L_D}$$ Equation 11.

and the Flatband Capacitance is:

$$C_{(FB)} = \frac{C_O C_D}{C_O + C_D} = \frac{C_O}{1 + \frac{L_D}{\frac{K_{Si} x_O}{K_O}}} .$$ Equation 12.

Once the Flatband capacitance is found, Vfb is obtained easily by finding the voltage that corresponds to Cfb. The flatband voltage is a very useful parameter. It is made up of

all the non-idealities in a MOS capacitor. This is seen in the following equation:

$$V_{FB} = \Phi_{MS} - \frac{Q_F}{C_O} - \frac{Q_M \gamma_M}{C_O} - \frac{Q_{IT}}{C_O}. \qquad \text{Equation 13.}$$

Of the four terms in the Flatband voltage equation, the last three are concerned with non-ideal charges in a MOS capacitor. They are described as follows:

Qf/Co - change in Vt due to the fixed oxide charge. (experimentally determined)

QmYm/Co - change in Vt due to total mobile ion charge in the oxide (exp. determined)

Qit/Co - change in Vt due to interfacial traps (experimentally determined)

The last three threshold voltage shifts are grouped together as deviations due to non-ideal charges in the oxide and on the oxide/silicon interface. There are ways of separating out each one, but in this work, they will be lumped into one variable Qeff/Co. The first term in equation 13 is the metal/semiconductor work function difference as mentioned earlier.

4.3. Square law theory

Although C-V measurements are very useful for characterization of a devise, in practical application, the four terminal MOS transistor is the workhorse of the industry and will be the focus of this work from here out. The following

discussion will give a brief description of the mechanics of a MOS transistor.

As mentioned in the C-V section of this work, there are three basic regions of operation in a transistor. They are Accumulation, Depletion and Inversion. In accumulation, the majority carriers in the channel are the opposite type of those in the S/D regions, making it impossible for current to flow under the channel. As the voltage changes and depletion sets in, the majority carriers are pushed away from the channel and a depletion region is formed. There are still no carriers to allow current. As inversion sets in, minority carriers, the same as majority carriers in the S/D, gather at the channel surface, and small currents begin to flow. Somewhere in the transition from depletion to inversion, the threshold voltage is defined. As inversion is in full swing, current flows freely and increases as the Drain voltage, Vds, is increased. The transistor is considered 'on' at this point. At a certain Vds, the current between the source and the drain saturates. This current is called I_{Dsat}, the saturation current and the Vds at which it occurs is V_{Dsat}. In an ideal device, as the drain voltage increases past V_{Dsat}, no more current flows. The previous discussion applies to standard devices with relatively large gate lengths (~>10um). Short channel effects will be discussed later.

One theory that is very basic and simple in the understanding of MOS transistors is the Square-Law Theory [3]. This theory relates the charge in the inversion layer due to the capacitance from the gate voltage and related oxide capacitance, to the Drain/Source current and voltage. The Square-Law Theory states two basic equations which relate Id and Vd. They are as follows:

$$I_D = \frac{Z u_n C_O}{L}\left[(V_G - V_T)V_D - \frac{V_D^2}{2}\right] \text{ for } 0 \le V_D \le V_{Dsat} \text{ and } V_G \ge V_T$$

Equation 14.

and

$$I_{Dsat} = \frac{Z u_n C_O}{2L}(V_G - V_T)^2 \qquad (V_D \ge V_{Dsat}).$$ Equation 15.

where Z is the transistor gate width L is the transistor gate length and Vt is the threshold voltage. Idsat is the saturation current at which an increase in Vds does not bring an increase in Ids. Using these two equations, a basic understanding of any given transistor can be found.

There is a second and more robust approach for calculating the channel current called the Bulk charge theory[4], but since only a surface look at these transistors will be done, the square law theory will be sufficient.

4.4. Vt Equations

All of the variables in the above equations are pretty straight forward so far except for calculation of the Threshold Voltage Vt. Several factors go into determining the Threshold Voltage. The general equation is as follows:

$$V_T = V_T' + V_{FB}.$$ Equation 16.

Since we have discussed Vfb earlier, we will look at Vt' here. Vt' is the threshold of an ideal device. The equation for this parameter is as follows:

$$V_T' = \frac{kT}{q}2U_F + \frac{q(N_A - N_D)}{K_S\varepsilon_O}X_O\left[\frac{2K_S\varepsilon_O}{q(N_A - N_D)}\frac{kT}{q}2U_F\right]^{1/2}.$$ Equation 17.

Or it can be written specifically for n and p channel devices:

$$V_T' = 2\phi_F + \frac{1}{C_O}\sqrt{4qN_AK_S\varepsilon_O\phi_F}$$ or n channel devices.

Equation 18.

$$V_T' = 2\phi_F - \frac{1}{C_O}\sqrt{4qN_DK_S\varepsilon_O(-\phi_F)}$$ for p channel devices.

Equation 19.

With all of the equations discussed so far, a good understanding of the operation of a long channel device can be obtained.

4.5. Short channel effects.

The previous discussion laid a groundwork for the fundamentals of MOS transistor technology. As industry strives to make smaller and smaller devices, several other problems are introduced. A very brief description of several short channel effects will be presented. The specific short channel effects that will be discussed here will be:

- Drain Induced Barrier Lowering (DIBL)
- Vt shifts
- Channel length modulation
- Sub Threshold Swing

4.5.1 Drain Induced Barrier Lowering

Drain Induced Barrier Lowering (DIBL) is a major cause for concern in the fabrication of state of the art short channel transistors[5]. DIBL is seen in the increase of drain current as a Drain voltage is applied. All transistors will have an increase of subthreshold current as the Drain voltage is increased. In short channels however, the increase of drain current is partly due to the fact that the voltage applied to the drain is helping to deplete the channel. This can be visualized by thinking of the depletion region under and next to the drain as intruding into and forming part of the channel depletion layer. The higher the voltage, the more the drain depletes under the channel. In practical applications, this is one of the driving factors in switching the operating voltage of some semiconductor devices from 5.0 volts to 3.3 volts. One graphical way of looking at DIBL is by plotting Subthreshold current (log scale) vs. Vds and no gate voltage applied. More

current will be in the channel for short channels then there will be for long channels.

4.5.2 Vt Shifts

The previous discussion dealt with the drain effects on the channel with a voltage applied. A second way of looking at the drain effects on a short channel is to look at the Vt shifts of short channel transistors with a very small Vds. As the channel gets shorter, the magnitude of the threshold voltage decreases. This can be explained by realizing that the depletion region made by the drain extends into and under the channel even though there is not a large voltage applied.

4.5.3 Channel length modulation

Channel Length Modulation is the first so called 'Short Channel' effect that was discovered[6]. Channel length modulation is seen in the fact that the Id-Vds curves at Idsat are not exactly flat, but actually have a positive slope. The mechanism for channel length modulation occurring is that as Vds increases above a certain voltage, Vds', at which the channel pinches off, a depletion region is formed between the drain and the channel. Since Vds is greater than Vds', and the voltage across the inversion layer remains fixed at Vds', there is a voltage drop across the depletion region equal to Vds-Vds'. As Vds increases, so must the depletion width.

The next step will be to look at the current in the channel. As seen from equation 14, the current, Id', in the channel during strong inversion is proportional to (const)/L. Even though Vds may increase above Vds', the voltage across the inversion channel length must remain at Vds'. This is the key

in determining the current in the channel. Now the channel is L-ΔL with a voltage drop of Vds'. The new current, Id, is also proportional to (const)/L-ΔL. The constant in both the previous equations is the same and depends on Vg. Combining these two equations gives:

$$I_D = I_D' \frac{L}{L - \Delta L} \qquad \text{Equation 20.}$$

With longer channels, the channel length doesn't relatively change much. In shorter channels, a large change in length is seen and therefore the current in the channel increases.

4.5.4 Sub Threshold Swing

The next short channel effect to be looked at will be the subthreshold voltage swing. This parameter describes the Volts/Decade current increase in the sub-threshold region. Even when the gate is turned off, there is a very small current through the gate. This is leakage current and is called the Sub Threshold Current. As the gate begins to deplete/invert the channel, this sub threshold current increases. The sub threshold swing is a measure of how much gate voltage is applied to induce a 1 decade current increase. Short channel devices will exhibit a smaller sub threshold swing than long channel devices due to the drain's influence on the channel depletion.

5. Alignment mark placement/process

One of the decisions that had to be made was how and where to place the alignment marks. Because of the nature of the E-Beam for exposure, a permanent straight walled feature had to be placed on the wafer. The MEBES I uses the E-beam to determine the location of the marks. As the beam is rastered across a smooth surface, the electrons are backscattered and a detector picks them up. If there is a vertical sidewall, the E-beam will scatter in many different directions and the detector will not detect any electrons. In this way, it can determine the position of the alignment marks. A diagram of an alignment mark used is shown in Figure 1.

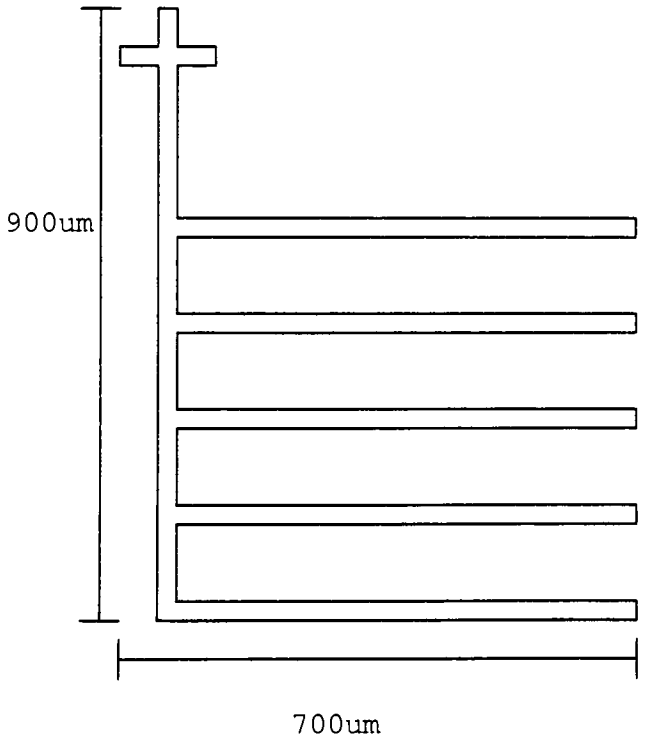


Figure 1

There are two basic methods for creating alignment marks. The first is a raised oxide bump. This is the easiest to process, but due to the large amount of HF cleans and etches, this did not seem very practical. The oxide bump would degrade with each damaging process step. The second is a pit etched in the silicon. This takes many more processing steps, but is a more robust alignment mark. The following is the process used for etching the alignment marks in the silicon.

1) Deposit Aluminum Thickness = 5022A

Volts: 330 V
Current: 10 A
Power: 3300 W
Time: 12 min.
Thickness: 5000 A

2) Alignment mark Photo

Coat:
Resist: HEBR213-2
Spin speed: 1500 RPM
Spin Time: 30 sec.

Expose:
Dose: 35uC

Develop:
Time: 1.5min.

3) Metal Etch

Acid: Phosphoric
Temp: 50 deg C
Time: 35 sec

4) Silicon Pit Etch

Power: 150 Watts
Pressure: 200mTorr
Gas 1: 30 sccm SF6

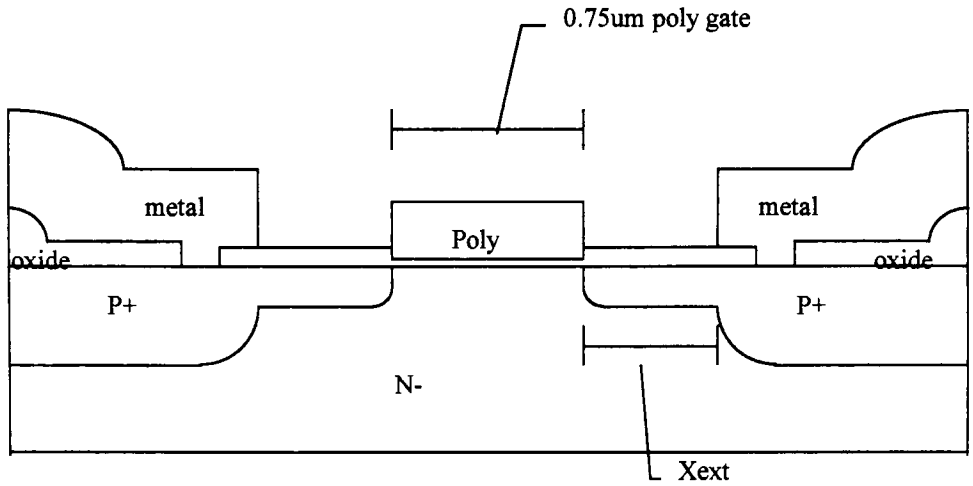
Gas 2: 9 sccm O2
Time: 3 min.

5) Metal Strip

Acid: Phosphoric
Temp: 50 deg C
Time: 1 min. (past clear)

The metal layer was used as an etch stop. The gases used to etch the silicon were SF6 and O2. Because there was so much oxygen in the etch, which will "ash" resist, and due to the thinness of the resist, it was determined to use aluminum as an etch barrier. The final etch pit thickness in the silicon was 2.5um.

6.0 Cross section and device dimensions



Cross section of 0.75 um Transistor.
Figure 2

Transistor dimensions

To get a full view of the transistor characteristics for this process, several transistor sizes were tried. The only two dimensions that were varied were the gate length and the length of the shallow Source drain regions (labeled Xext in Figure 2.). Varying the gate lengths made it possible to look at short channel effects and varying the shallow Source/Drain regions guaranteed that a device would work, and if alignment was good, made it possible to see a very efficient device. There were twelve different transistors fabricated and they are as follows in Table 1.

Shallow S/D length	Gate Length
2.00 um	0.75 um
2.00 um	1.00 um
2.00 um	1.25 um
2.00 um	2.00 um
2.00 um	3.00 um
2.00 um	5.00 um
5.00 um	0.75 um
5.00 um	1.00 um
5.00 um	1.25 um
5.00 um	2.00 um
5.00 um	3.00 um
5.00 um	5.00 um

Table 1.

7.0 Photolithography Scheme

There was one very large limiting factor in determining the type and thickness of resist to be used. The MEBES I at R.I.T. was made to supply a 20KeV E-Beam, but only 10KeV was available while processing was going on. This made it impossible to use more than 2000A resist. Unlike an energy wave exposure, the E-Beam has a very limited depth profile.

8. Layout design of the standard device.

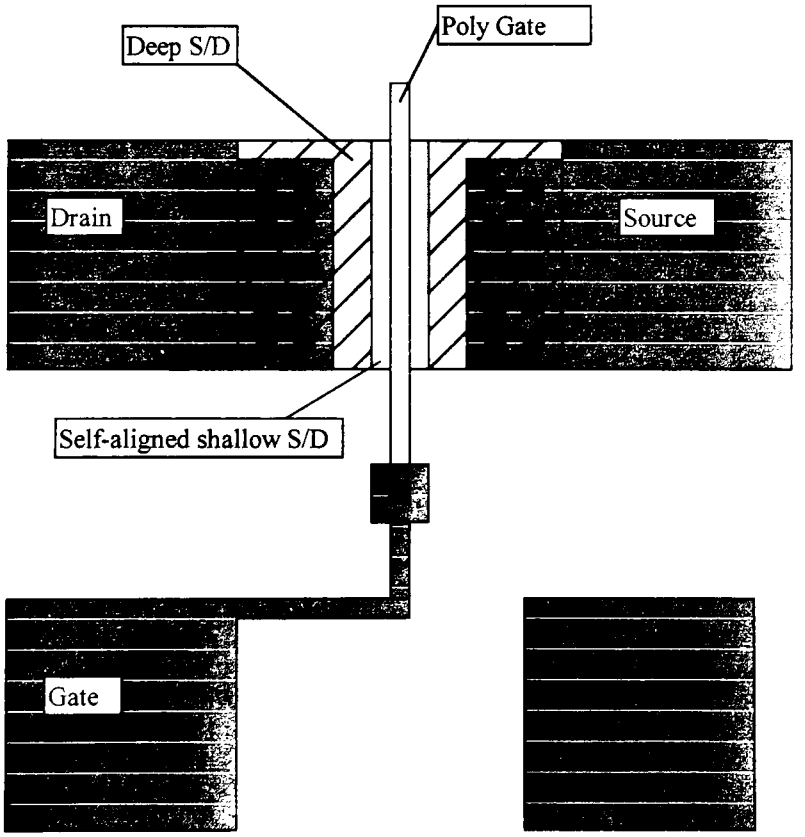


Figure 3.

9. Miscellaneous Process considerations

There were four process considerations made when this devise was planned. They were:

- PMOS/NMOS selection
- Very large width transistors
- Boron diffusion problems
- Metal spiking -- D/S junction depth

The decision to go with PMOS over NMOS rested with one major consideration. The question of non-idealities in the gate oxide was the driving factor. The purpose of this thesis was to produce a working submicron transistor as efficiently as possible. Since most non-idealities in the gate oxide tend to shift the threshold voltage of a transistor in the negative direction, it was decided to go with PMOS which has a naturally negative threshold voltage. In this instance, a shift negative would not make the devise fail, only make it impractical. If NMOS was used, a positive shift could have permanently impaired the transistor from working.

One drawback of using PMOS rather than NMOS was the fact that Boron diffuses very fast, and has a tendency to be attracted to oxide. The fact that it has a high diffusion rate made the S/D activation a big consideration. The S/D's had to be activated, but in the process, if the boron diffused under the gate too much, the short channel devices would have shorted. To accomplish both the activation and the low diffusion, a large dose was implanted (5e15a/cm3) and a short low temperature activation was performed (850deg for 40min).

The question of transistor width was put to rest by deciding to use a very wide transistor. Even though the gate length was sub-micron, the width was 100um. The purpose behind

this choice was to guarantee that if the transistor worked, it would have enough drive to get some reasonable characteristic curves.

The last major consideration was the Metal spiking issue. To obtain working submicron PMOS transistors, a very shallow junction had to be made. But if the junction was to shallow, the metal that made contact to the S/D would spike through the junction and cause a short to the well. It was decided to use a deep S/D for the metal contact and an LDD to contact the channel. The way the LDD was done in this process was to create the deep S/D, then align the gate in between them and implant a self aligned LDD.

10. Process

The following is the process used to create the transistors:

1) Wafer Start

Start with P-Type <100> wafers doped with a resistivity of 5-15 ohm-cm.

2) Clean

RCA Clean

3) Initial Pad Oxide

Time: 8 min.
Temp: 1100 deg. C
Gas: Dry O2

4) NWELL Implant

Dopant: Phosphorous
Energy: 50 KeV
Dose: 5.0e12

5) Pad oxide etch

7:1 BOE etch till dewet.

6) Field oxide growth

Time: 150 min.
Temp: 1100 deg C.
Gas: Dry O2

7) Active area Photo

Coat:

HMDS: 4000RPM/40 sec.
Resist: HEBR213-1

Spin speed: 7000 RPM

Spin Time: 30 sec.

Expose:

Dose: 9uC

Develop:

Time: 4 min.

8) **Active Area Etch**

7:1 BOE etch till dewet.

9) **Resist Strip**

10) **Heavy Drain Photo**

Coat:

HMDS: 4000RPM/40 sec.

Resist: HEBR213-1

Spin speed: 7000 RPM

Spin Time: 30 sec.

Expose:

Dose: 9uC

Develop:

Time: 4 min.

11) **Boron Heavy Drain Implant**

Dopant: Boron

Energy: 100 KeV

Dose: 1.0e15

12) **Resist Strip**

13) **Clean**

RCA Clean

14) Gate Oxide

Time: 60 min.
Temp: 950 deg C.
Gas: Dry O2

15) Gate thick. etch

50:1 HF
210 sec.

16) Poly Deposition

3000 Ang. Poly Dep.

17) Poly Doping implant

Dopant: Boron
Energy: 45 KeV
Dose: 1.0e15

18) Poly etch Photo

Coat:

HMDS: 4000RPM/40 sec.
Resist: SAL601
Spin speed: 6000 RPM
Spin Time: 60 sec.

Expose:

Dose: 5uC

PEB:

Time: 1min
Temp: 115 deg C

Develop:

Developer: SAL622
Time: 4-5 min. till clear

19) Poly Etch

Power: 100 Watts
Pressure: 50mTorr

Gas 1: 30 sccm SF6
Gas 2: 3 sccm O2
Time: 45 sec.

20) Resist Strip

21) Source/Drain Implant

Dopant: BF2
Energy: 60 KeV
Dose: 5.0e15

22) Clean

RCA Clean

23) Contact Oxide/Boron Activation

Time: 40 min.
Temp: 850 deg C.
Gas: Dry O2

24) Contact Cut Photo

Coat:

HMDS: 4000RPM/40 sec.
Resist: HEBR213-1
Spin speed: 7000 RPM
Spin Time: 30 sec.

Expose:

Dose: 9uC

Develop:

Time: 4 min.

25) Contact Cut Etch

Acid: 7:1 BOE
Time: 1 min.

26) Metal Deposition

Power: 2.6Kw
Volts: 3.7KV
Current: 700mA
Time: 12 min.
Thickness: 8000A

27) Metal Etch Photo

Coat:

HMDS: 4000RPM/40 sec.
Resist: HEBR213-1
Spin speed: 7000 RPM
Spin Time: 30 sec.

Expose:

Dose: 9uC

Develop:

Time: 4 min.

28) Metal Etch

Acid: Phosphoric
Temp: 47 deg C
Time: 52 sec

29) Alloy

Time: 20 min.
Temp: 425 deg C
Gas: N2

30) [illegible]

11. Results and discussion

Figures4-7 were obtained using the Spreading Resistance profile technique (SRP). They are doping concentration profiles taken from resistance vs. depth measurements.

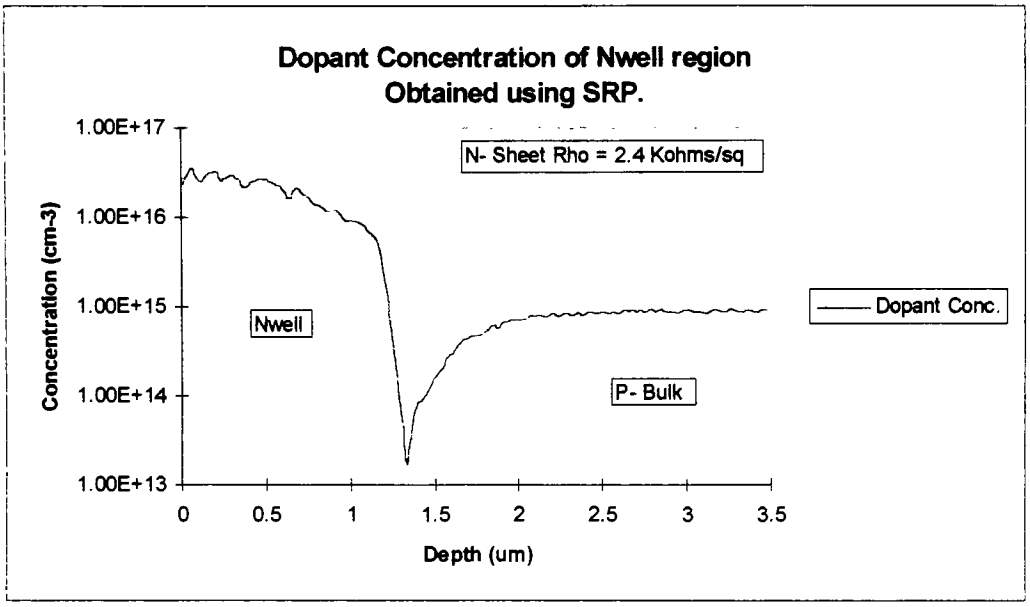


Figure 4.

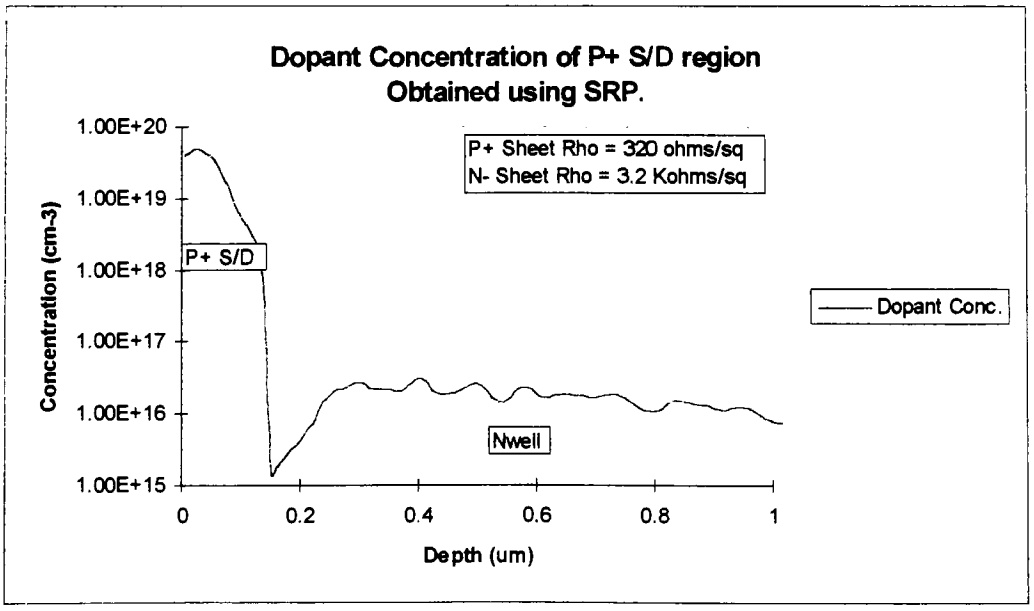


Figure 5.

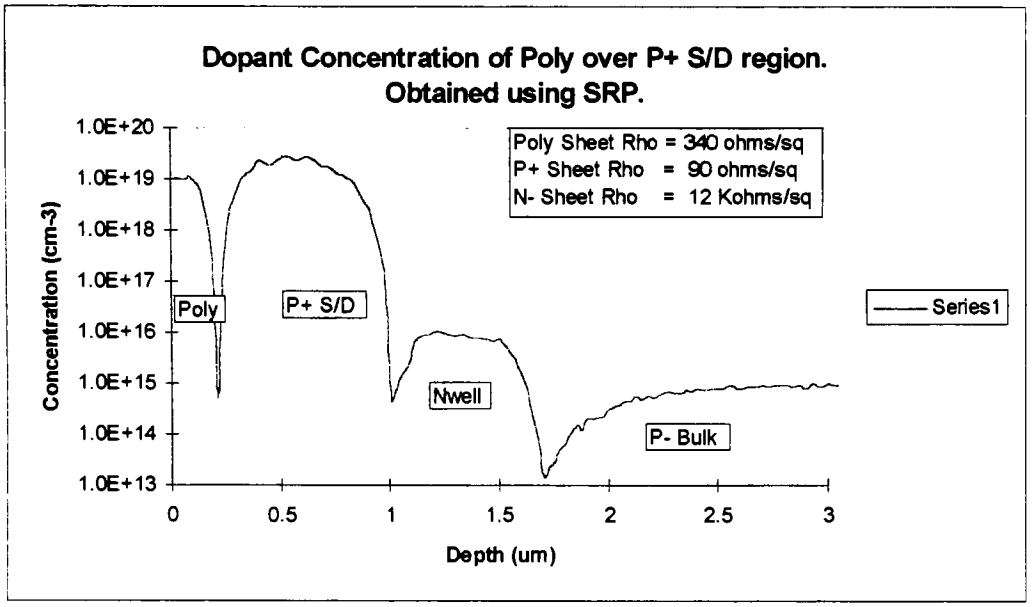


Figure 6.

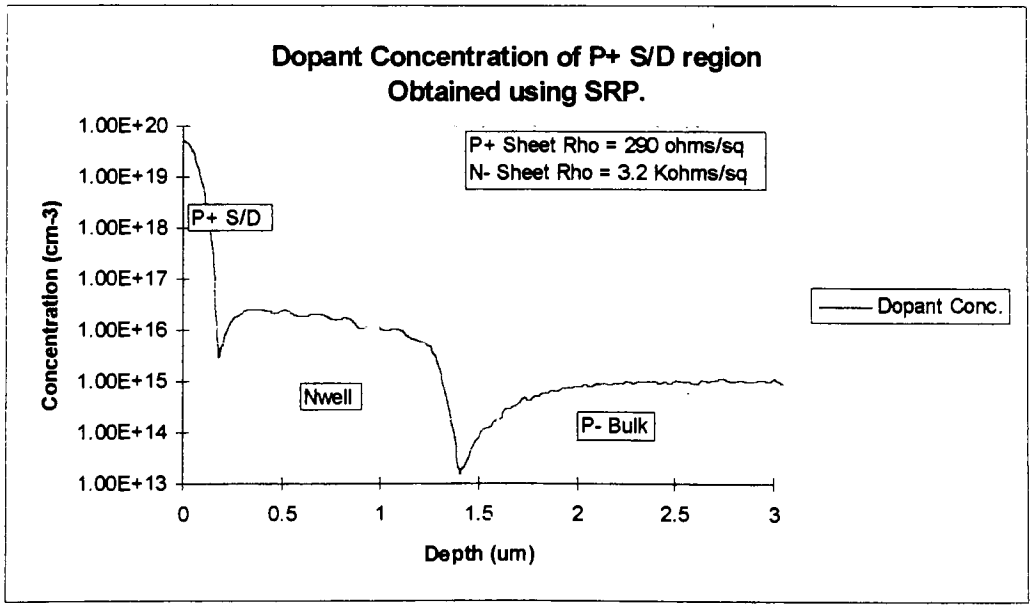
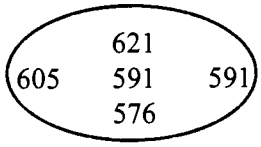


Figure 7.

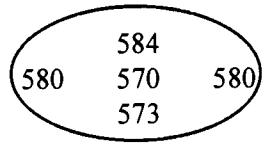
11.1. Actual Process Results.

Sacrificial Pad Oxide:

Wafer D10: Avg=597

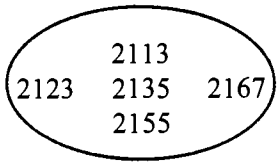


Wafer D8: Avg=577A

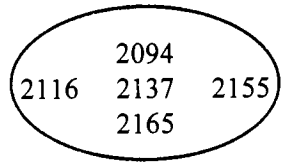


Field Oxide:

Wafer C3: Avg=2139A

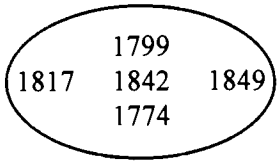


Wafer D10: Avg=2133A

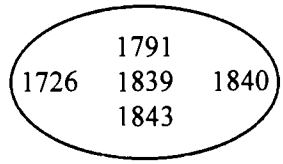


Field Oxide Before Gate :

Wafer D8: Avg=1816A

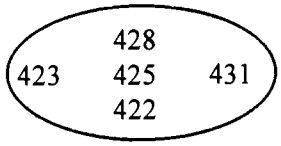


Wafer D10: Avg=1808A

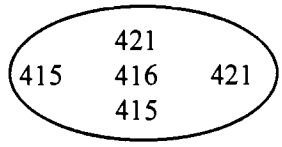


Gate Oxide (Before Etch) :

Wafer D10: Avg=426A

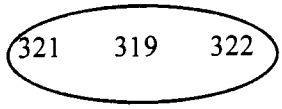


Wafer D8: Avg=418A



Gate Oxide (After Etch):

Wafer D10: Avg=321A



Wafer D8: Avg=328A

Poly Thickness on Dummy:

2752 2758 Average=2759A
2744 2782

11.2. Device parametrics

The following results were taken from the SRP graphs above along with the actual process results and calculated parameters from these results.

Na (poly gate) = 1e19 A/cm3
Nd (well) = 3e16 A/cm3

$\Phi_{Bulk} = -386V$

$\Phi_{Gate} = +537V$

$\Phi_{MS} = +.923V$

Cox = 11.5 μF/cm^2

$u_{Peff} \approx 180\, cm^2/_{VS}$

The first area to examine in this thesis will be the C-V data. Figure 8 is a C-V plot of a 316x316um square of metal on top of poly over 300 A gate oxide.

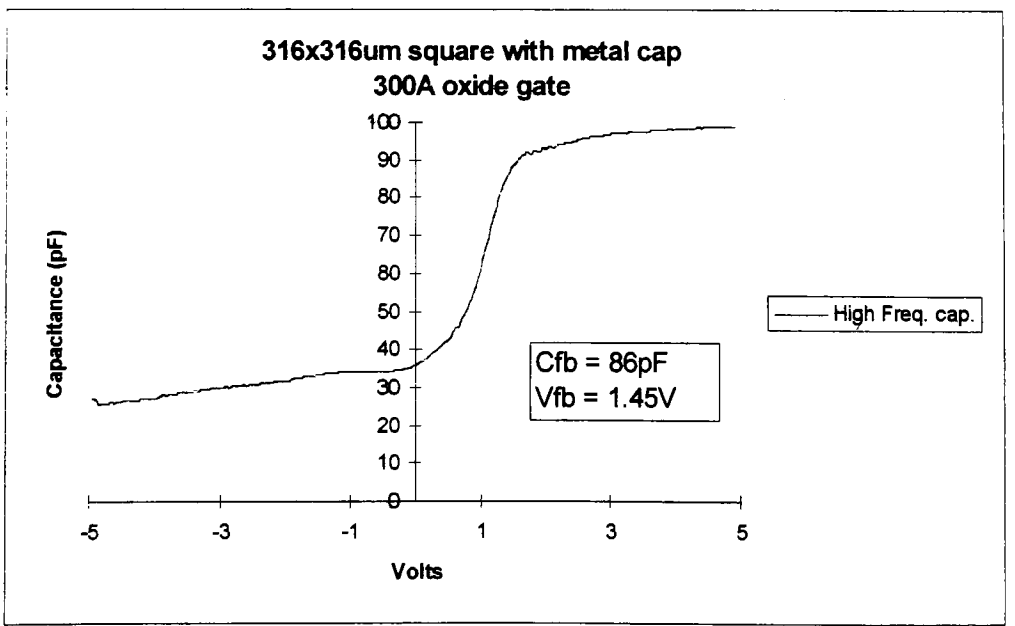


Figure 8.

The calculated C_{Omax} for this size transistor is 115pF. The maximum capacitance taken from this graph using the high frequency curve is 98.8pF. One explanation for this could be the downward shift of this curve due to any series resistance involved in the measurements. If the series resistance could be calculated, and the curve shifted up, this would decrease Vfb by a small amount. Because of the difficulty in measuring the Low frequency CV curve, the results will be used from the high frequency curve, keeping in mind this disparity.

The next parameter to extract is the Flatband capacitance Cfb.

After several calculations, the Flatband capacitance was obtained:

Cfb = 86pF

The corresponding Vfb was

Vfb = 1.45

The end result for obtaining Vfb is to determine Neff, the interface charge states. This was done in two different ways and both were compared as follows:

Qss/Cox from Vfb side

Vfb = 1.45 V

Φms = 0.93 V

Qss/Cox = -0.52 V

Neff = -3.8e11

Qss/Cox from Vt side

Vt = -.2 V

Vt'(calc) = -1.58 V

Φms = 0.93

Qss/Cox = -0.45 V

Neff = -3.3e11

These results are quite close. The one thing to note is that Qss/Cox is a negative value. This means that there are negative charge sites in the oxide. One factor that be effecting this is that there could be boron that diffused into the oxide. This has been seen to shift the threshold voltage in the positive direction for thin oxide gates[7].

The next set of results will be the threshold voltage measurements. Figure 9 shows the Drain to Source current vs. the gate voltage for the .75µm transistor. Extrapolating the curve to get an x-intercept gives a threshold of -.15 volts.

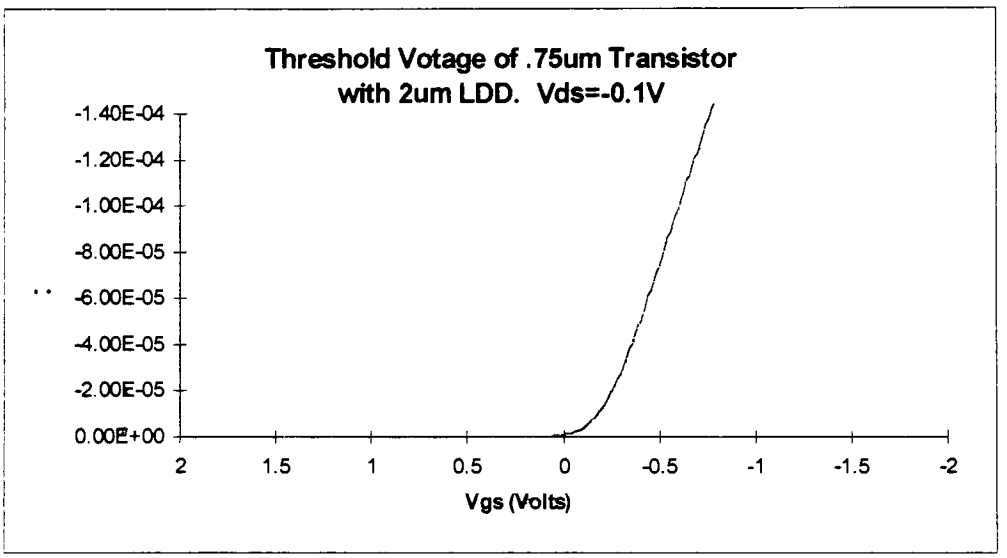


Figure 9.

Figure 10 shows Vd vs. Ids curves for the .75um transistor.

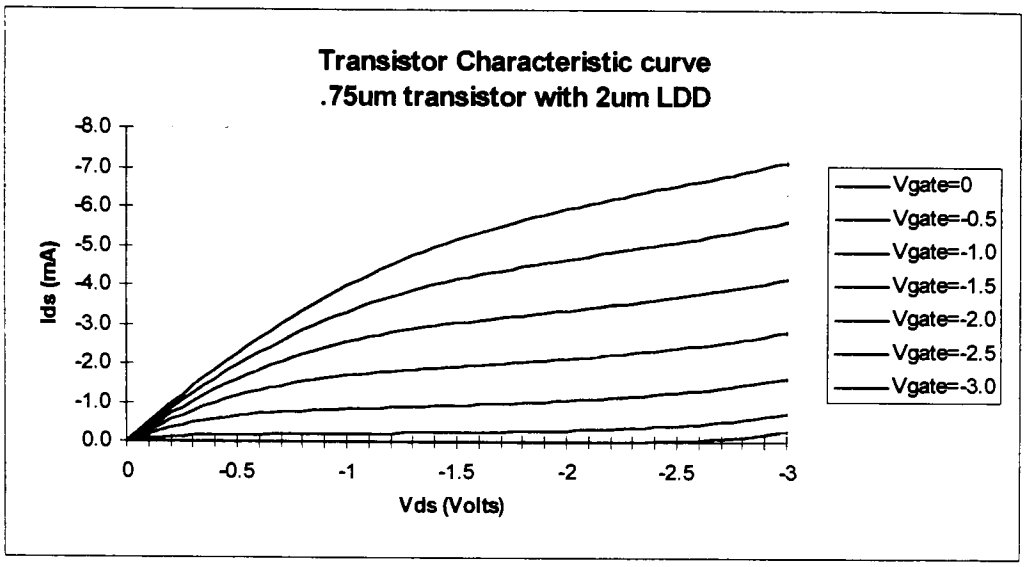


Figure 10.

Applying the Id equation below to this transistor yields the following results:

Vt = -.15V
Z = 100um
L = .75um
un = 18 um^2/VnS
Co = 1.15fF/um^2
Vg = -3.0V
Vd = -.2

$$I_D = \frac{Z u_n C_O}{L}\left[(V_G - V_T)V_D - \frac{V_D^2}{2}\right] \text{ for } 0 \le V_D \le V_{Dsat} \text{ and } V_G \ge V_T$$

Id = -1.52mA

Interestingly enough, the raw data gives a value of -0.96mA. Although not exact, the current is relatively close.
A table of results is given to show the expected vs. measured results. One thing to keep in mind is the fact that the square law theory was used here and short channel effects are not involved in these calculations.

Channel Length	Vt	Vds	Vg	Id meas.	Id calc.
0.75	-.15 V	-.2 V	-3.0 V	1.52 mA	0.96 mA
1.00	-.15 V	-.15 V	-0.5 V	0.11 mA	0.07 mA
1.25	-.15 V	-.7 V	-3.0 V	2.74 mA	2.84 mA
2.00	-.2 V	-.4 V	-2.0 V	0.73 mA	0.66 mA
3.00	-.2 V	-.3 V	-1.5 V	0.33 mA	0.13 mA
5.00	-.3 V	-.2 V	-3.0 V	0.17 mA	0.19 mA

Table 2.

11.3. Drain Induced Barrier Lowering - DIBL

The first short channel effect to look at is the Drain induced barrier lowering. This can be seen in a couple of ways. First, figure 11 shows the sub threshold current vs Vds. for varying channel lengths. This graph as mentioned earlier shows DIBL.

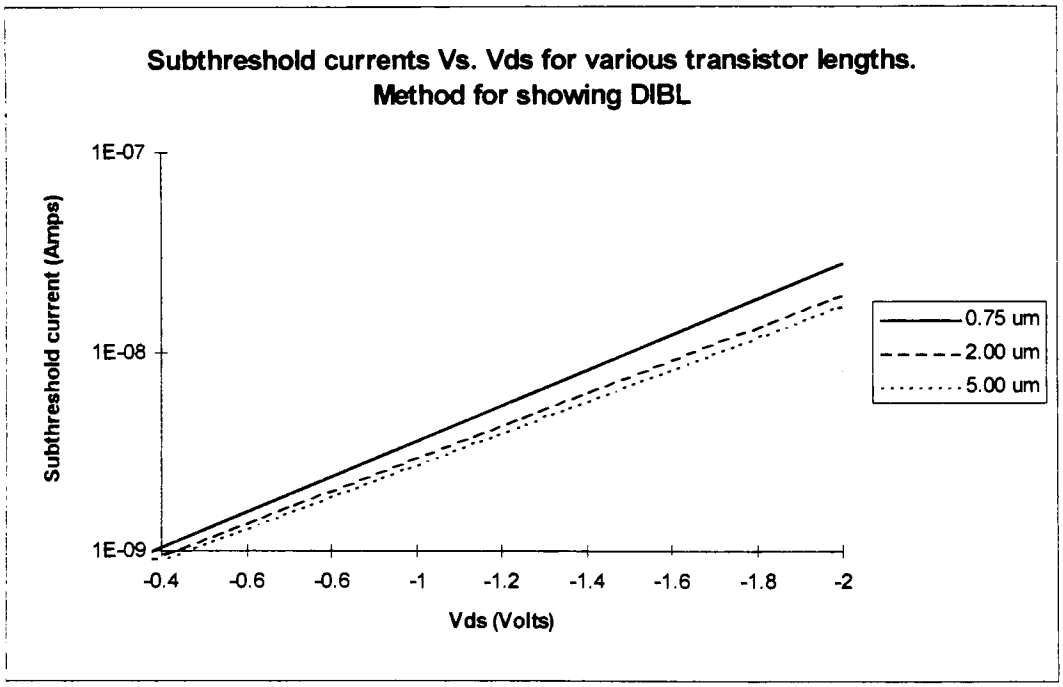


Figure 11.

As can be seen, the current of the 0.75μm transistor is larger than the 2 and 5 μm transistors.

11.4. Vt shifts

A second way to describe the effect of a short channel is through Vt shifts with transistor gate length. This effect is seen with a very small Vds as seen from figure 12. Since Vds=-0.1 is such a small voltage, it can be assumed that the majority of the effect on Vt's is coming from the built in drain depletion width extending into and under the channel. This aides the gate in depleting/inverting the channel, therefore leading to a lower threshold voltage.

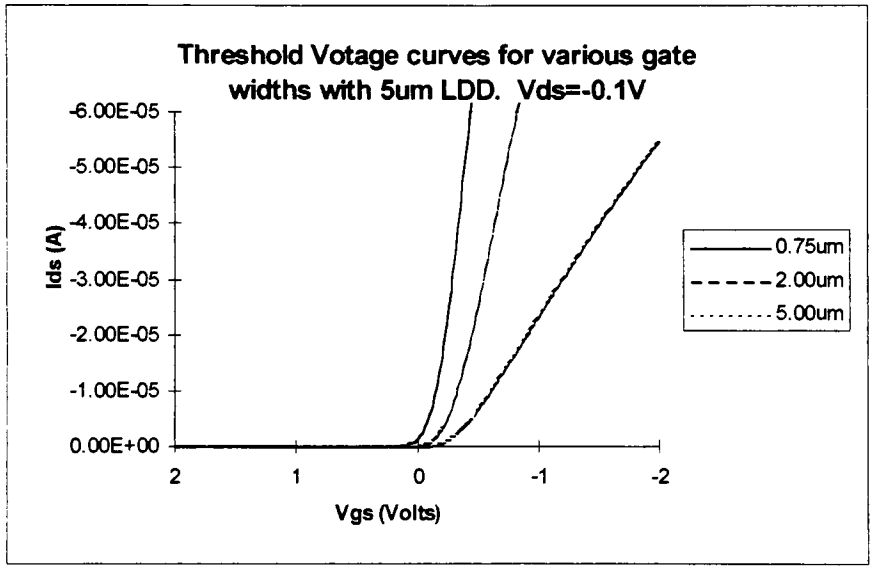


Figure 12.

The shift seen here is between .05 and .1 volts. As the gate length increases, the threshold voltage also increases (in the negative direction).

11.5. Channel Length Modulation

The next short channel effect that will be demonstrated by actual measurements will be channel length modulation. As mentioned earlier, channel length modulation can be best seen on the Id-Vds curves as a slope in the line after Idsat has been reached. Figure 13 shows channel length modulation.

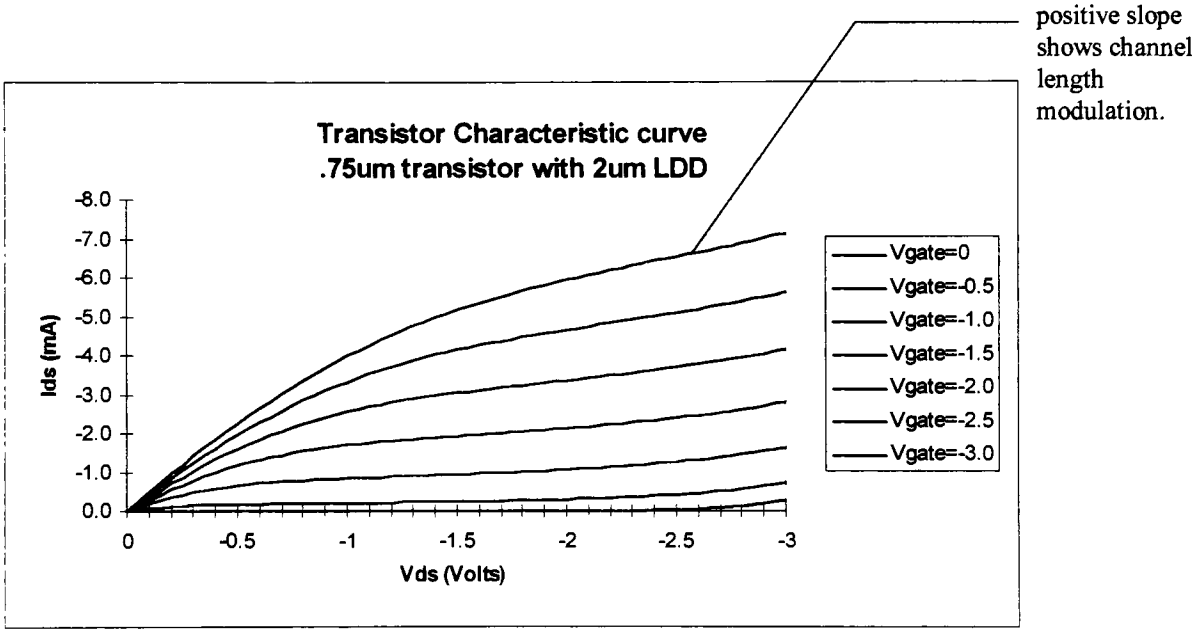


Figure 13.

Caution must be made when trying to describe channel length modulation from graphs like the one above. It has been shown earlier that the drain has an effect on channel current through DIBL. Although channel length modulation can be seen in the slope of the above curves, it must be noted that some of the current increase can be explained by other effects. The separation of DIBL and channel length modulation can be done, but it will not be looked at in this work.

11.6. Sub Threshold Swing

The last short channel effect to be looked at will be the subthreshold voltage swing. The results of this effect have been tabulated belowand were taken from Figure 14.

Gate Length	Sub Threshold swing
0.75 um	0.13 V/decade
2.00 um	0.14 V/decade
5.00 um	0.16 V/decade

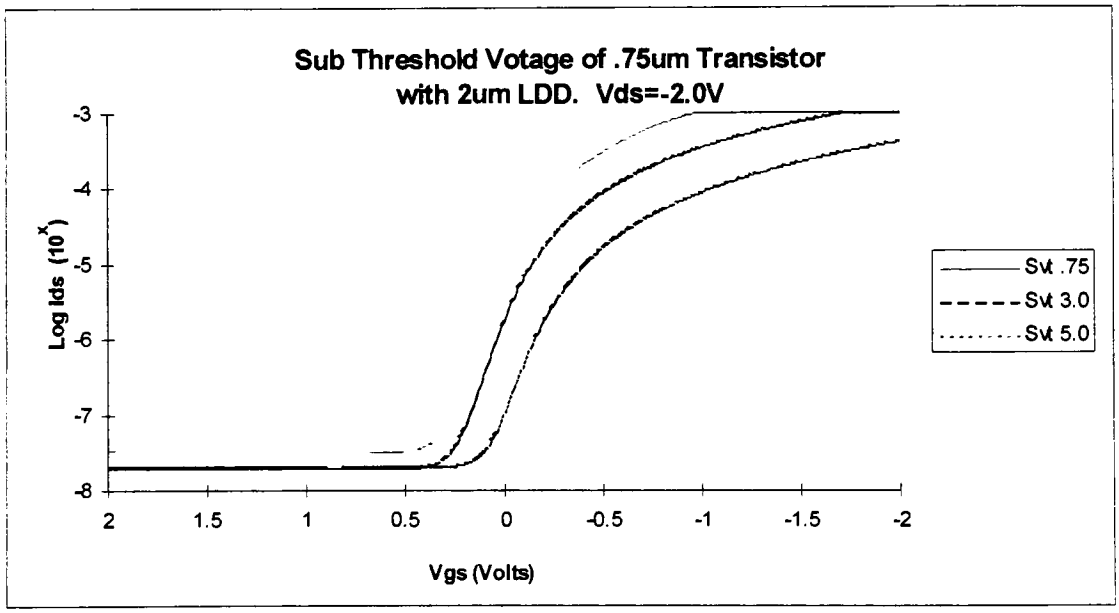


Figure 14.

12. Conclusions - Future work

A working sub-micron PMOS transistor was created using Direct Write Lithography. In addition, several short channel transistor effects were briefly discussed.

As mentioned in the introduction, there is one major drawback to Direct Write E-Beam Lithography. It is the thruput issue. An example of the poor thruput is that one wafer at the poly level took 90 minutes to expose.

There are several things that can be done to improve upon this process. They are as follows:

- Combine Stepper lithography with Direct write to speed up the lithography steps.

- Characterize and understand the negative charge states calculated for the apparent Vt shifts.

- Experiment with short channel width transistors.

- Try using N+ poly doping to keep the Vt's higher.

- Use these transistors in practical applications.

13. References

1. P.J. Coane et al. "Electron beam/Optical Mixed Lithography at Half-Micron Ground Rules", Microelectronic Engineering 5 (1986) Elsevier Science Publishers B.V. (North Holland) p133.

2. Robert F. Pierret, Modular Series on Solid State Devices Volume I: Semiconductor Devices, Second Edition Addison-Wesley Publishing Company, Reading Massachusetts. p66.

3. Robert F. Pierret and Gerold W. Neudeck, Modular Series on Solid State Devices Volume IV: Field Effect Devices, Addison-Wesley Publishing Company, Reading Massachusetts. p89.

4. Robert F. Pierret and Gerold W. Neudeck, Modular Series on Solid State Devices Volume IV: Field Effect Devices, Addison-Wesley Publishing Company, Reading Massachusetts. p90.

5. Savvas G. Chamberlain and Sannasi Ramanan, "Drain-Induced Barrier-Lowering Analysis in VLSI MOSFET Devices Using Two-Dimensional Numerical Simulations," IEEE Transactions on Electron Devices. Vol. ED-33, No. 11, November 1986. p1745.

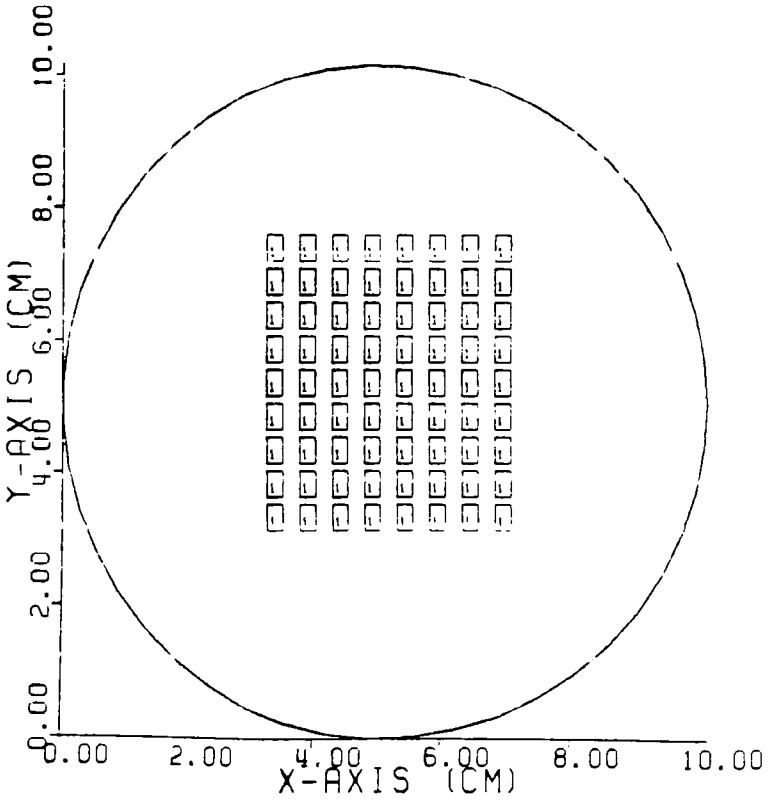
6. Yanis P. Tsividis, Operation and modeling of the MOS Transistor, McGraw-Hill, New York. p169.

7. L.K. Han et al., "Highly Suppressed Boron Penetration in NO-Nitrided SiO2 for p+-Polysilicon Gated MOS Device Applications," IEEE Electron Device Letters, Vol, 16, No 7, July 1995. p319.

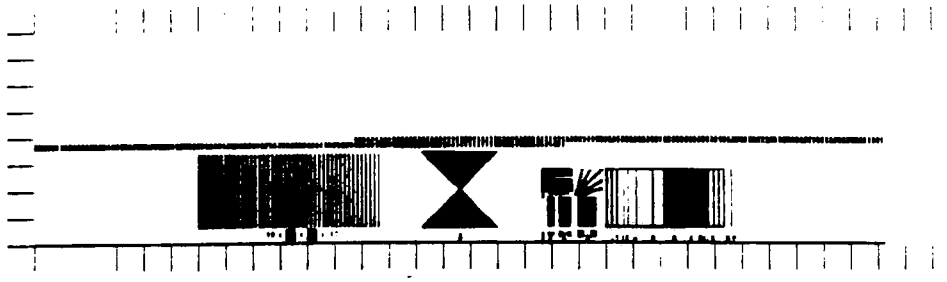
Appendix A - Miscellaneous Mebes Work

Wafer layout

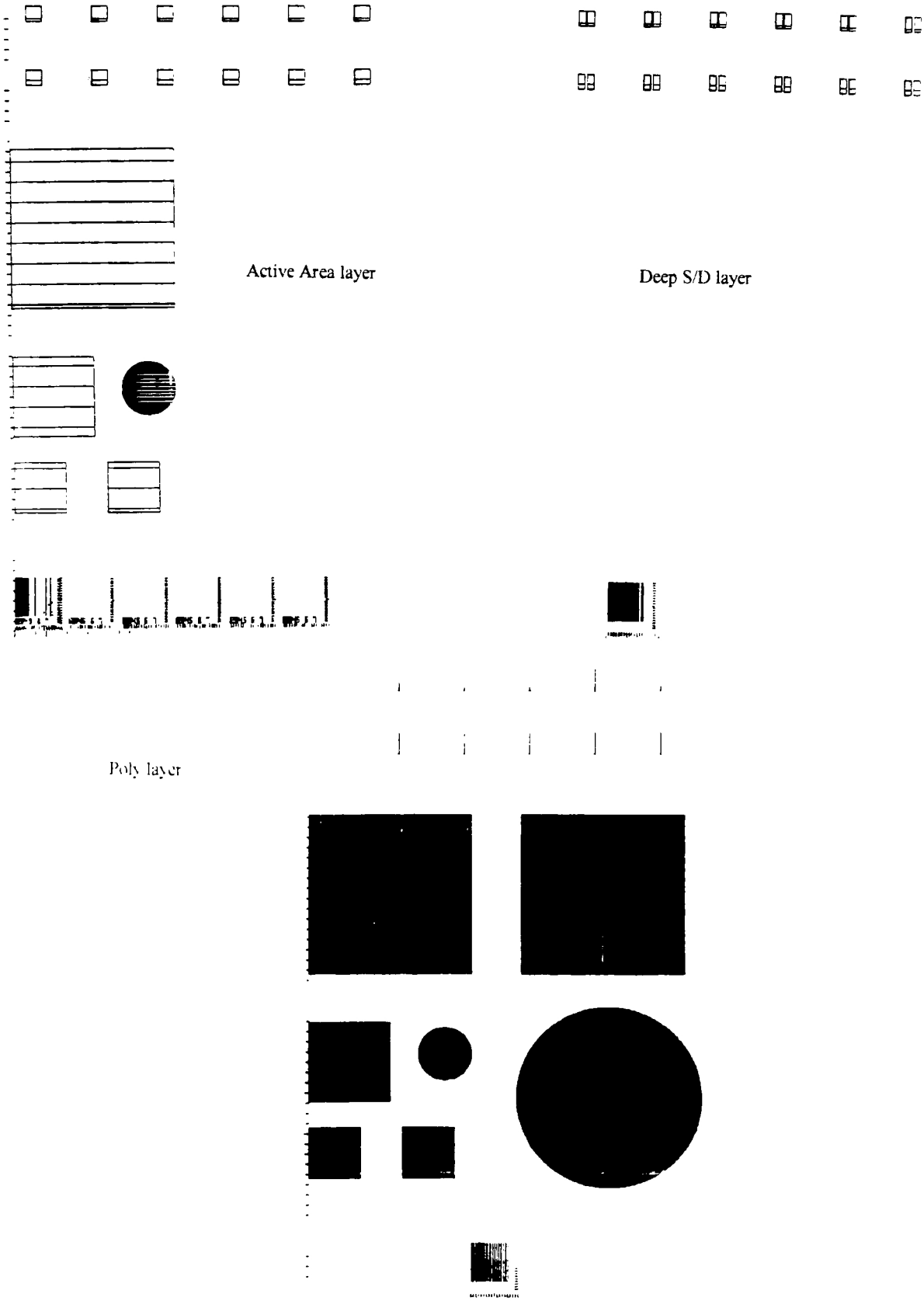
The following is the transistor layout across the wafer. I placed an 8x9 grid of transistor/capacitor sets on the wafer for plenty of testing locations to test.

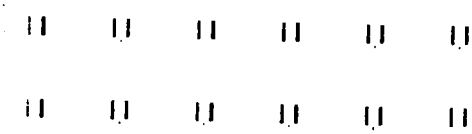


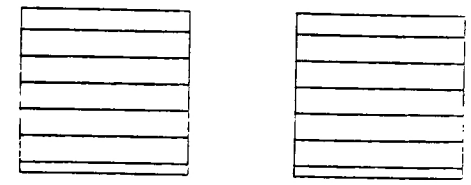
I also used the following pattern to do a dose matrix before each photo step. This was a standard design used to check several lithography characteristics. By exposing a 2x8 matrix of this pattern with 16 different doses, I was able to obtain the proper exposure for each step.



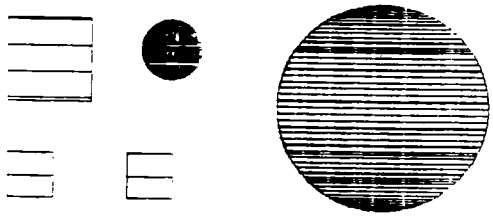
** Interesting note: The dose for exposure over metal does not change from that over other films. This is only logical since electrons don't reflect like light, but my instinctive training using steppers had to be disregarded for this experiment.

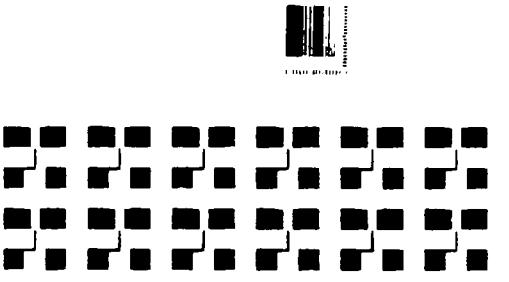

Active Area layer
Deep S/D layer
Poly layer





Contact Cut layer





Metal layer

```
SLICE EDIT,13,    TED:KIM.JB
*  EMCR670 MEBES 1 ELECTRON BEAM LITHOGRAPHY EXPERIMENT
*  NEGATIVELY WORKING CHEMCALLY AMPLIFIED RESIST-SAL603(SHIPLEY)
*  EXPOSURE OF .5UC/CM2 IN 8 STEPS
*!
*! GROUP COMMANDS
*!
SCALE 1
*!
*! ALPHA, RETICLE, REPEAT AND SIZING COMMANDS
*!
*! OPTION COMMANDS
OPTION          SA=20, AA=.5, BA=.5,    VA=10
*!
*! TITLE AND ORIENT COMMANDS
*!
*! CHIP AND ROWS COMMANDS
*!
CHIP N1,
$   (1,    L173634-01-02, RC=1) *! COUNT 20  SIZE (5000,10000)
ROWS 40000/28300
*!
CHIP N2,
$   (1,    L173634-01-02, RC=2) *! COUNT 20  SIZE (5000,10000)
ROWS 40000/34700
*!
CHIP N3,
$   (1,    L173634-01-02, RC=3) *! COUNT 20  SIZE (5000,10000)
ROWS 40000/41100
*!
CHIP N4,
$   (1,    L173634-01-02, RC=4) *! COUNT 20  SIZE (5000,10000)
ROWS 40000/47500
*!
CHIP N5,
$   (1,    L173634-01-02, RC=5) *! COUNT 20  SIZE (5000,10000)
ROWS  40000/53900
*!
CHIP N6,
$   (1,    L173634-01-02, RC=6) *! COUNT 20  SIZE (5000,10000)
ROWS 40000/60300
*!
CHIP N7,
$   (1,    L173634-01-02, RC=7) *! COUNT 20  SIZE (5000,10000)
ROWS 40000/66700
*!
CHIP N8,
$   (1,    L173634-01-02, RC=8) *! COUNT 20  SIZE (5000,10000)
ROWS 40000/73100

*!
END
```

Mebes Job Decks

```
SLICE MARK.4.     ALIGNMENT MARK DEPOSITION
* DEPOSITION OF TYPE TWO ALIGNMENT MARKS
* FOR THE JUMP DEVICE FOR MARK KLARES THESIS
*!
*! GROUP COMMANDS
*!
SCALE 1
*! OPTION COMMANDS
OPTION SA=10, AA=.25  BA=.25,  VA=.0
*!
CHIP ACTIVE, (1,SILMARK-00-07  RC=30) *! ACTIVE AREA OPENING
ROWS 33520/29140
ROWS 33520/74860
ROWS 79240/52000
END
```

Alignment mark [illegible]

```
SLICE MARK.4.  JOB DECK FOR JUMP DEVICE
* JOB FILE INCLUDING ALL FIVE LAYERS
* OF THE JUMP DEVICE FOR MARK KLARES THESIS
*!
*! GROUP COMMANDS
*!
SCALE 1
*! OPTION COMMANDS
OPTION SA=10, AA=.25  BA=.25,  VA=.0,F1,2,3,4,5=5,R3
FID 5,29140,33520.74860,33520 52000.79240
MARKTYPE 5, (A,1)
*!
CHIP ACTIVE,
$    (1,G123932-MK-01. RC=12) *! ACTIVE APEA OPENING
$    (2,G123932-MK-02. RC=14) *! META. CONTACT OPENING (IMPLANT)
$    (3,G123932-MK-03. RC=5) *! POLY PATTERNING
$    (4,G123932-MK-04. RC=11) *! CONTACT CUT LAYER
$    (5,G123932-MK-05. RC=5) *! METAL LAYER
ROWS 33520,9,5000/34520;39300.7,5000
END
```

Job deck for each of the [illegible]

Appendix B - E Beam Resist Data

New Product Announcement

Olin Hunt

Waycoat® HEBR-214 Positive Electron Beam Resists

Available in 1 quart and 1 gallon bottles
Compatible with most commercially available processing equipment

Description

Waycoat® HEBR-214 series positive resists are novolak based and aqueous developable. They have been optimized for electron beam exposure while maintaining the processing advantages of novolak based resists. These resists are sensitive to ultraviolet light, X-rays, and electron beams making them suitable for MIX N' MATCH lithography. Waycoat HEBR-214 resists spin at different coatings ranging from 0.25, 0.5, and 1.0 micron. They offer some unique advantages over conventional e-beam resists.

Benefits include:

- *Excellent coating characteristics*
- *Aqueous developable*
- *Ease of processing*
- *High resolution—0.25 micron*
- *Excellent plasma etch resistance*
- *Good sensitivity*
- *High contrast*
- *Low sodium content*
- *Batch to batch consistency*

Process Conditions

The data represented was generated with HEBR-214 in the following process.

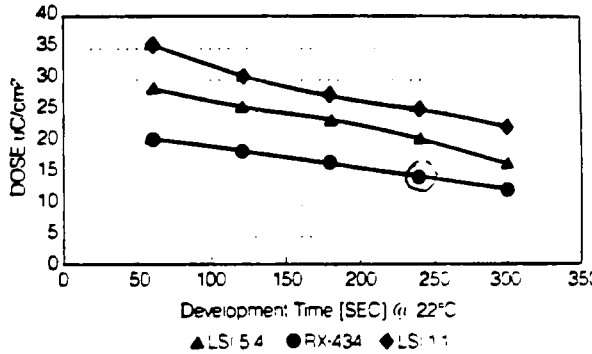
Priming
HMDS immersion for 30 seconds (wafers only)

Coating
Resist spinner 5000 rpm, 30 seconds for various thicknesses

Soft Bake
100°C ± 2°C, 30 minutes, convection oven or 110°C for 50 seconds on Track

Exposure:
Depending on requirements. See Figure 1.

Figure 1 Dose vs Development HEBR-214



Developer
Waycoat® LSI (5.4)
Experimental RX-434

Time
LSI (5.4) 120 seconds
RX-434 240 seconds

Method
Immerse in developer without agitation at 22°C ± 1°C

Rinse
DI Water, 1 minute, blow dry

Sensitivity – 20KeV Wafer – 10KeV mask
24 μC/cm² wafer LSI (5.4)
14 μC/cm² wafer RX-434
7 μC/cm² mask RX-434

Substrate preparation

The substrates must be clean and dry to insure coating quality, optimum adhesion and process consistency. The recommended minimum dehydration bake for wafers is 300°C for 2 hours in a convection oven. Before coating chrome mask blanks must be cleaned with solvent, ultrasonic, or scrubbing techniques.

Resist Filtration

Resists have been filtered and packaged in a Class 10 clean room facility. For best results, point of use filtration is also recommended. Use Millipore Millex 0.22μ Teflon® membrane filters for syringes.

Priming

For wafers, the use of Waycoat* Adhesion Promoter (HMDS) is recommended to insure good adhesion of HEBR-214 resists HMDS is *not* recommended for chrome blanks

Spin Coating

WAYCOAT* HEBR-214 resists can be applied by manual or automated techniques Relation between spin speed and film thickness is given in Fig 2 The following is a typical cycle

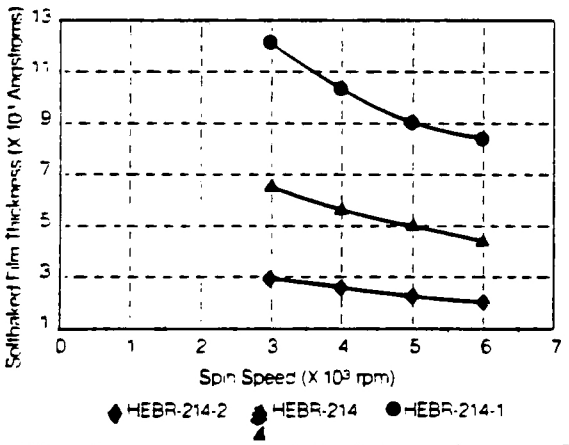
Manual

Dispense 3 to 4 ml of resists on static wafer Spin dry at 5000 rpm for 30 seconds

Auto

Dispense 3 to 4 ml of resist on static wafer Spread for 3 seconds at 600 rpm Accelerate at 6000 rpm/sec Spin dry for 30 seconds at 5000 rpm

Figure 2 Spin Speed vs. Film Thickness HEBR-214



Soft Bake Prebake

The purpose of this bake is to remove residual solvents left after coating and to promote adhesion between resist and coated substrate

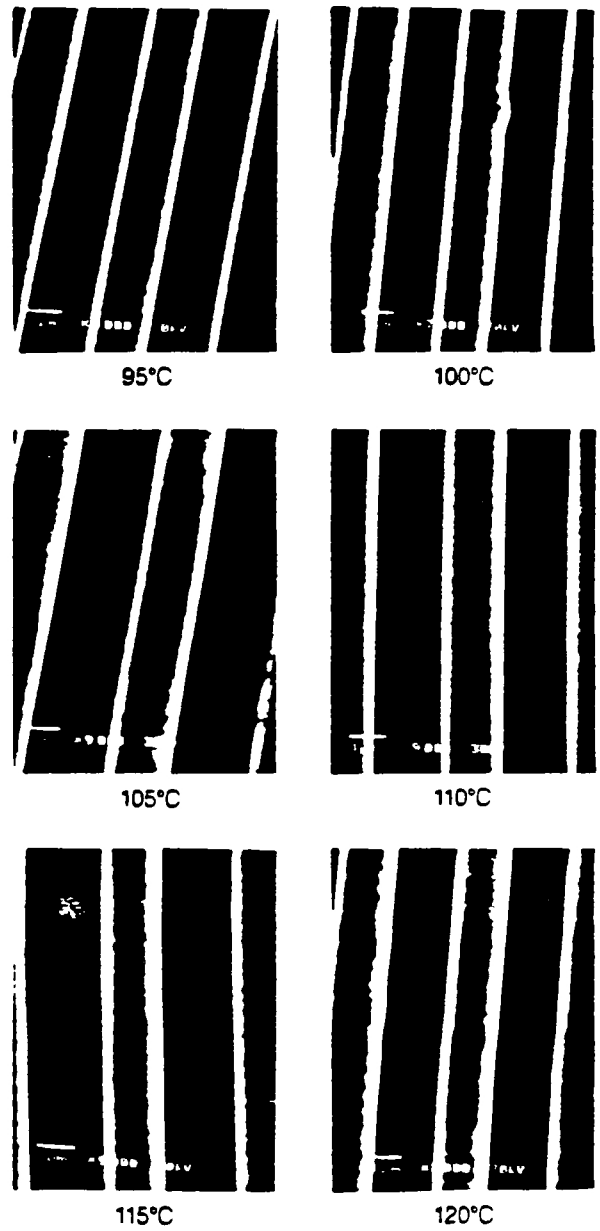
Waycoat HEBR-214 can be soft baked using a convection oven or a track hot plate system Higher soft bake temperatures provide higher sensitivity, and improve adhesion

Waycoat HEBR-214 resists can be prebaked in a convection oven at 100° to 105°C for 30 minutes or on a hot plate at 110°C for 50 seconds

Recommendations:

Method	*Time*	*Temperature*
Convection	30 minutes	100°C ± 5°C
Hot plate	40 to 60 seconds	100°C ± 5°C

The following SEM micrographs processed at indicated temperatures for soft bake.



Exposure and Sensitivity

HEBR-214 resists are specially designed and formulated for electron beam exposure and due to their sensitivity to X-rays and UV radiations, the resists can also be imaged with these exposure systems. However, with the widespread variation in exposure systems, specific exposure recommendations cannot be provided. The performance of these resists is process dependent since exposure conditions, developer type, developer concentration, developing technique, and time influence performance Sensitivities of 14 to 24 uC/cm² @20KeV can be achieved depending on the resolution requirements, film thickness retention, and the e-beam exposure tool Some typical values are given in Table 1

TABLE 1
Typical contrast and film thickness loss

Resist	Method	Time (sec)	Sensitivity (uC/cm²)	Contrast	Film Loss (Angstroms
	Immerse	120	24 0	2 00	720
	Spray	120	20 5	1 60	920
	Puddle	120	18 0	1 24	1200
HEBR-214	Immerse	240	14 0	3 00	300

Figure 3 Dose vs Development HEBR-214

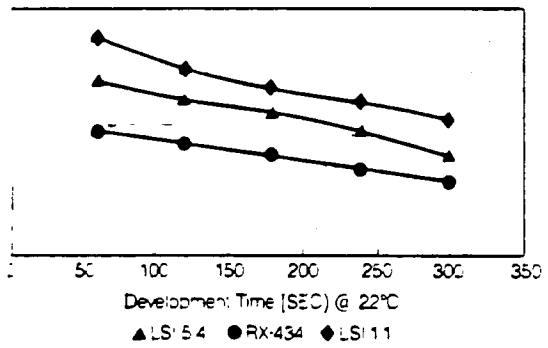
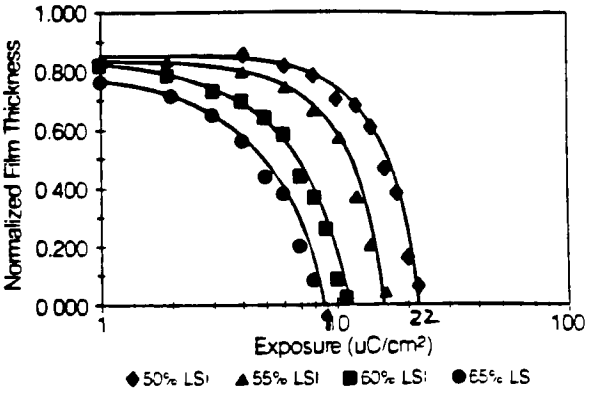
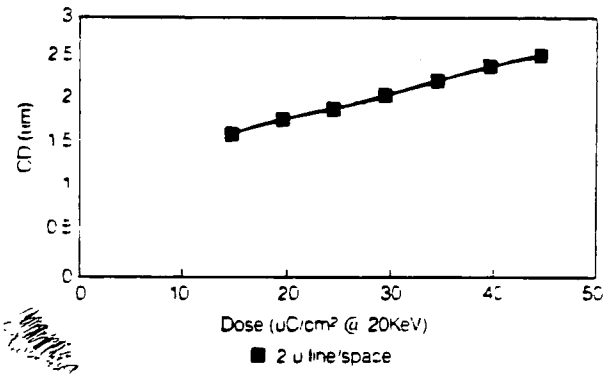


Figure 4 Characteristic Curve HEBR-214 60 sec. immersion





Post Bake

Substrates can be post baked in a convection oven at 100° to 115°C for 30 minutes to obtain maximum adhesion and image quality. Post bake also improves the plasma etch resistance. Waycoat HEBR-214 can also be deep UV cured by standard techniques to improve thermal stability.

Plasma Etch Resistance

Just like any other novolak based resist, HEBR-214 resists offer excellent plasma etch resistance and are superior to conventional e-beam resists such as PBS, COP, EBR-9, FBM-120, etc. Typical values are given in Table 2.

Table 2

Resist	*Etch Rate (Ang Sec)*	*Conditions*
HEBR-214	21	Omnietch 10000
EBR-9	73	Power 50 Watts
FBM-120	37	Pressure 2.1 Torr
PBS	140	Gas Argon 10% CF_4 75%
SiO_2	26	Flow rate Argon 400 sccm CF_4 82 sccm

Resist
Thickness 1.5 µm
Dev Time 100 seconds

Substrate
1st Layer Silicon
2nd Layer Silicon Oxide

Stripping

Waycoat HEBR-214 can be stripped using the OLIN HUNT Microstrip™ 2001 or oxygen plasma if it has been post baked. Without post bake, the resist can be easily removed with an acetone solvent.

Technical Data

	HEBR-214	*HEBR-214-1*	*HEBR-214-2*
Solids (%)			
Minimum	20.75	26.75	13.75
Maximum	21.25	27.25	14.25
Viscosity (cps)			
Minimum	6.2	13.50	3.50
Maximum	7.2	14.50	4.50
Water Content			
Minimum	0.0	0.00	0.00
Maximum	0.5	0.50	0.50
Filtration	0.22 micron (absolute)		

Certificates of Analysis are available for each production batch and indicate tests performed and the results.

Safe Lights

Coated substrates and open bottles should be handled under yellow lights only.

Packaging

Waycoat HEBR-214 is supplied in one US quart and one US gallon bottles.

Safety, Storage and Handling

See Material Safety Data Sheet for details.

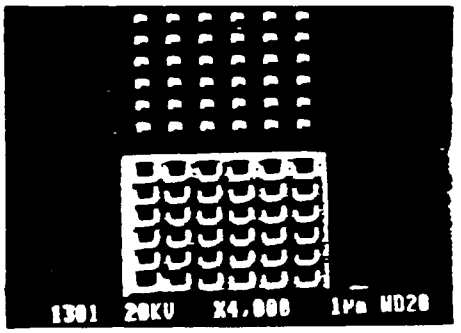
Product Information

Material	*Thickness*	*Packaging*	*Catalog No.*
HEBR-214	5000A	1x1 Quart	844076
		1x1 Gallon	844136
HEBR-214-1	10000A	1x1 Quart	844078
		1x1 Gallon	844079
HEBR-214-2	2500A	1x1 Quart	844080
		1x1 Gallon	844081
LSI DEVELOPER		4x1 Gallon	838264
MICROSTRIP™ 2001		4x1 Gallon	843957
WAYCOAT® HMDS		4x1 Gallon	844019
RX-434 DEVELOPER		4x1 Gallon	844094

Figure 6 SEM Micrographs

Waycoat® HEBR-214 used with an Electron Beam System @ 20 KeV. HEBR 214-exhibits submicron contact holes and islands at 0.75 and 0.50 micron (top SEM micrograph) Bottom SEM micrograph exhibits submicron resolution of 0.25 micron lines.

Substrate: Silicon
Spin Coat: 1.0 micron
Exposure: Jeol E-Beam System
Develop: LSI (5:4) 240 seconds
Measurement: Jeol SEM



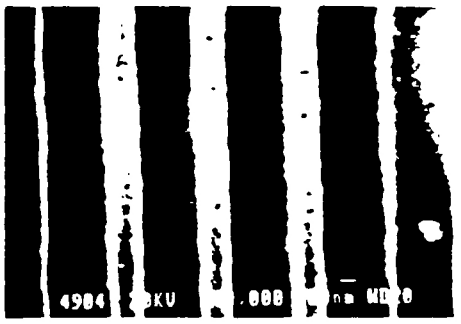


Figure 7 SEM Micrographs

Waycoat® HEBR-214 used with an X-Ray System. HEBR-214 exhibits submicron lines, spaces and islands at 0.75, 0.35 and 0.2 micron.

Substrate: Silicon
Spin Coat. 1.0 micron
Exposure: Hampshire Instrument X-Ray System
Develop. LSI (5:4) 180 seconds
Measurement: ISI SEM

MICROPOSIT® SAL® 600 E-BEAM PROCESS

DEVELOPMENTAL SHIPLEY ADVANCED LITHOGRAPHY

MICROPOSIT SAL600 E-BEAM PROCESS, utilizing the negative tone MICROPOSIT SAL601™-ER7 E-BEAM RESIST, has been designed to maximize the throughput and resolution capabilities of electron beam lithography. Its attributes of high sensitivity, greater process tolerance, and easy alignment result in efficient use of expensive equipment. Because this resist is novolac based and aqueous alkaline developable, it is non-swelling, and thus provides greater resolution and critical dimension control. Companion developers include the metal ion free MICROPOSIT SAL MF®622 DEVELOPER, or, for use on aluminum substrates, MICROPOSIT SAL660® DEVELOPER. Ideal use of the SAL600 E-BEAM PROCESS is in direct-write applications

Reduced Writing Time

- Approximately 7 $\mu C/cm^2$ sensitivity for 90% film retention (@ 20 keV)
- Productivity gains

Negative Tone But Non-Swelling

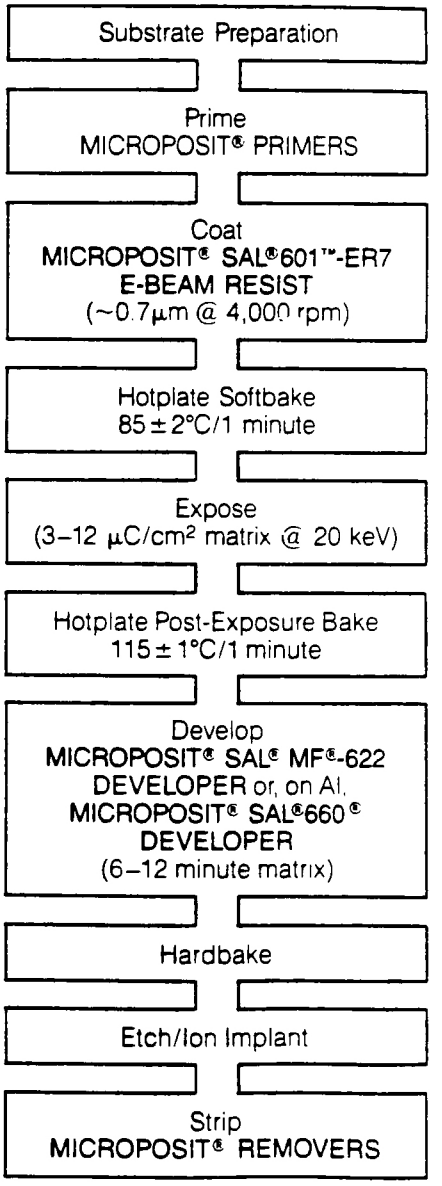
- Improved resolution
- Greater CD control
- Good clean out of fine lines

Aqueous Alkaline Development

- Metal ion free MICROPOSIT SAL MF-622 DEVELOPER or, for use on aluminum substrates, MICROPOSIT SAL660 DEVELOPER

Excellent Post-Development Processing

- Structural integrity under routine ion implanting, dry etching, and wet etching
- Thermal stability up to 200°C
- Plasma resistance equivalent to other MICROPOSIT positive photoresists



Patent pending

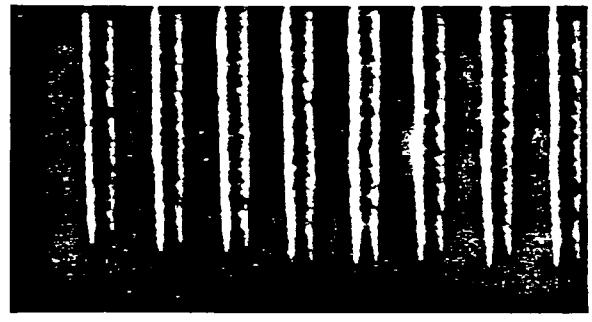
MICROPOSIT SAL601-ER7 E-BEAM RESIST will be shipped only in strict compliance with COCOM and DOD regulations

Under the Toxic Substance Control Act, MICROPOSIT SAL601-ER7 E-BEAM RESIST is restricted for commercial use in the manufacture of integrated circuits and photomasks

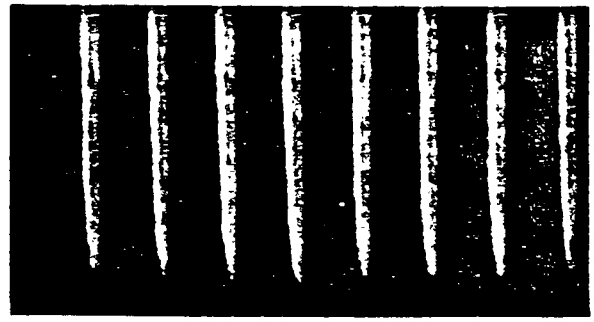
MICROPOSIT SAL 600 E-BEAM PROCESS

0.5μm L/S

0.4μm L/S



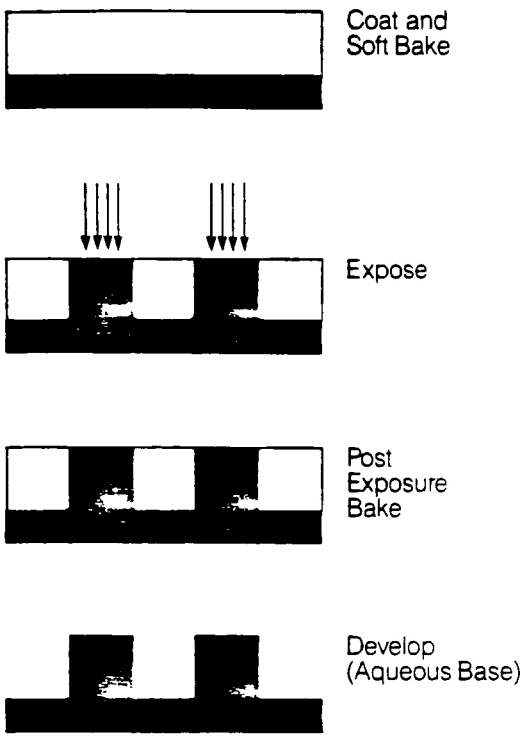
0.3μm L/S



0.2μm L/0.4μm S

The above scanning electron micrographs are representative of typical resolution and side-wall angle achieved with the MICROPOSIT SAL600 E-BEAM PROCESS.

Process Overview



MICROPOSIT SAL601-ER7 E-BEAM RESIST contains a novolac resin, a crosslinking agent, and a radiation sensitive acid generator. Upon exposure, a small amount of acid is generated. Then, during the post-exposure bake, the free acid catalyzes the crosslinking of the exposed areas.

I. Overview

MICROPOSIT SAL600 E-BEAM PROCESS, utilizing the negative tone MICROPOSIT SAL601-ER7 E-BEAM RESIST, is up to ten times faster than standard diazoquinone based novolac systems. Because this resist is novolac based, it is non-swelling, and unlike other E-beam processes, the MICROPOSIT SAL600 E-BEAM PROCESS includes aqueous alkaline development. The result is excellent post-development processing characteristics: ion implant masking, plasma and wet etching integrity, and thermal stability up to 200°C.

As with any process, image quality and reproducibility is influenced by many variables. These include substrate type, film thickness, electron beam energy, prebake conditions, postbake conditions (i.e. temperature, time, type of heating source), developer parameters (i.e. concentration, agitation, development time), and pattern geometries. As part of the MICROPOSIT SAL600 E-BEAM PROCESS, the metal ion free MICROPOSIT SAL MF-622 DEVELOPER is recommended (or, for use on aluminum substrates, MICROPOSIT SAL660 DEVELOPER). Note that to achieve optimal results, the post-exposure bake is the most critical process step to control.

II. Instructions for Use

A. Dehydration Bake/Prime

MICROPOSIT SAL601-ER7 E-BEAM RESIST can be patterned with good adhesion over a variety of substrates such as aluminum, polysilicon, gold, and oxide. Vapor phase priming with MICROPOSIT PRIMER is recommended for achieving maximum adhesion. If liquid phase priming is used, MICROPOSIT PRIMER TYPE P is recommended.

With the use of either MICROPOSIT PRIMER or MICROPOSIT PRIMER TYPE P, the substrates should first be baked at 200°C for 30 minutes and then cooled to ambient 18°–25°C immediately prior to priming in order to obtain maximum process reliability.

Note that the post-exposure bake and the hard-bake step also improve adhesion.

B. Application

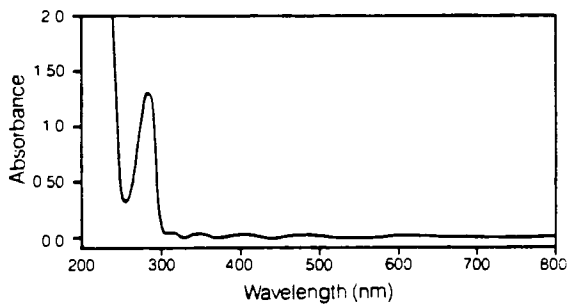
MICROPOSIT SAL601-ER7 E-BEAM RESIST is designed to produce low defect coatings both within a wafer and wafer-to-wafer using a variety of different processing parameters. The following coating process is recommended as a starting point:

Dispense:	Static for 3–5 seconds
Ramp:	Maximum acceleration
Spin Speed:	3000 to 6000 rpm
Spin Time	30 to 60 seconds

Unlike typical optical resists, the SAL601-ER7 E-BEAM RESIST has virtually no absorbance at 300 to 800nm, as depicted in Figure 1. Therefore, there is no need for special handling under yellow lights.

Figure 1

Absorbance of SAL601-ER7 E-BEAM RESIST



C. Edge Bead Removal

MICROPOSIT EBR-10 is recommended for removing resist build-up occurring at the edge of wafers during spinning. The formulation has been specified to be free of EGMEA, acetone, and xylene. EBR-10 can be used with most coating equipment designed to include an edge bead removal process.

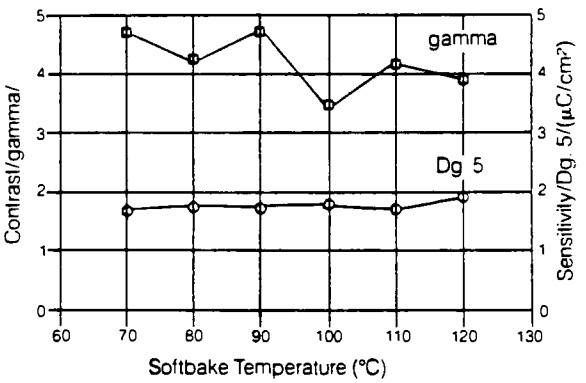
D. Softbake

Resist process latitude is not a strong function of softbake conditions. Figure 2[1] displays the sensitivity (Dg.5) and contrast (gamma) values obtained from normalized thickness remaining versus exposure doses plotted as a function of softbake temperatures (1 minute; hotplate). Dg.5 refers to the dose required for 50% film retention. Gammas were calculated by taking the slope of a line tangent to the contrast curve at the 0% retention point.

As shown, both sensitivity and contrast remain fairly constant over the softbake range of 70°C to 120°C. Thus, a suggested softbake is 85°C for 60 seconds on a hotplate prior to exposure. Alternatively, a 70°C to 80°C for 30 minutes in a forced air convection oven bake may be employed.

Figure 2

Sensitivity and Contrast vs. Softbake Temperature



The substrates were exposed on a JEOL JBX-6AII vector-scan variable shaped beam, direct-write machine at 20 keV. The hotplate post-exposure bake was at 105°C for 2 minutes. Immersion development was in MICROPOSIT MF-312 CD-27 DEVELOPER for 10 minutes.

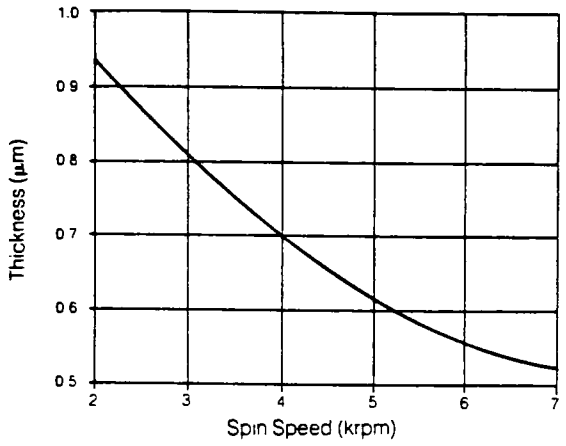
E. Resulting Spin Speed Curve

MICROPOSIT SAL601-ER7 E-BEAM RESIST should be spin-coated at 3000–6000 rpm for 30 to 60 seconds for optimum uniformity. Figure 3 illustrates the relationship between film thickness and spin speed.

[1] H. Liu (Hewlett Packard Co.) and M. DeGrandpre & W. Feely (Rohm & Haas Co.) "Characterization Of A High Resolution Novolac Based Negative E-Beam Resist with 4μC/cm² Sensitivity," presented at the 1987 3-beams conference: Electron-beam, X-ray, & Ion beam.

Figure 3

Thickness vs. Spin Speed



F. Exposure

MICROPOSIT SAL601-ER7 E-BEAM RESIST has been demonstrated to respond to electrons ranging in energy from 10 to 50 keV. The optimum dose for the resist is influenced by a number of factors such as substrate type, electron energy, resist thickness and pattern geometry. A typical lithographically useful dose for defining 0.5 µm and larger features is 7 µC/cm^2 at 20 keV for a 0.7 µm film on silicon substrates. Users must determine the appropriate dose for their specific applications. A 3 to 12 µC/cm^2 matrix of exposure doses is recommended to characterize the resist for each unique process.

The resist does not require a post-exposure cure period in a vacuum. Immediately following exposure, the patterned wafer can be removed for subsequent process steps. For maximum control and latitude the exposed resist should be post-exposure baked within a 4 hour period after removal from the exposure tool.

With typical processing, the interwafer linewidth variation has been found to be <0.005µm (one sigma variation for 56 chips/wafer). Similarly, the intrawafer linewidth variation has exhibited a one sigma value of <0.006µm (56 chips/wafer × 12 wafers)[2]

G. Post-Exposure Bake

This key step requires a well controlled uniform hotplate (± 1°C over the surface) for optimum results. If the bake is not well controlled, critical dimensions across the wafer may vary unacceptably. For a post-exposure bake of 60 sec. on a hotplate, the sensitivity of an isolated gap to variations in postbake temperature was found to be 0.02µm/°C, for temperatures ranging from 110° to 125°C. Similarly, the sensitivity to post-exposure bake time (at a temperature of 115°C) was found to be 0.003µm/sec. for times ranging between 54 and 63 sec[3]

A bake of 115°C/60 sec. on a hotplate with a vacuum chuck is suggested as a good starting point. A 105° to 125°C matrix at varying hotplate bake times is recommended to optimize the process.

After the bake step, relief images are visible on the resist surface. The exposed areas decrease in thickness by 5% to 10% depending on the aggressiveness of the bake. Generally, a vacuum chuck hotplate provides superior process control and is recommended over convection oven processing. If an oven must be used, 7 minutes at 105°C is recommended.

H. Development

Contrast and resolution increase with longer development times. Extended development time helps clear areas of the resist partially exposed by scattered electrons (proximity effects). Consequently, longer development times (6 to 12 minutes) provide higher contrast and resolution. Early data in the use of MICROPOSIT SAL601-ER7 E-BEAM RESIST has been obtained with Shipley MICROPOSIT MF-312 DEVELOPER[4] For high resolution patterning, Shipley has formulated a special metal ion free developer, MICROPOSIT SAL MF-622 DEVELOPER to be used for 6 to 12 minutes in the immersion mode. Alternatively, MICROPOSIT SAL660 DEVELOPER can be used if metal attack becomes a problem. Contrast values greater than 3 are obtained routinely with these development conditions as shown in Figures 4 and 5.

[2] M. DeGrandpre, K. Graziano, S. Thompson (Rohm & Haas Co.), H. Liu (Hewlett Packard Co.) and L. Blum (Shipley Co. Inc.), "High Resolution, Novolak Based Negative Tone Electron Beam Resist" presented at the 1988 SPIE Symposium on Microlithography proceedings to be issued

[3] Ibid

[4] H. Liu (Hewlett Packard Co.) and M. DeGrandpre & W. Feely (Rohm & Haas Co.) "Characterization of A High Resolution Novolac Based Negative E-Beam Resist With 4µC/cm^2 Sensitivity," presented at the 1987 3-Beams Conference Electron-beam, X-ray & Ion beam

Figure 4

Normalized Thickness vs. Dose
MICROPOSIT SAL MF-622 DEVELOPER
(10 minute immersion)

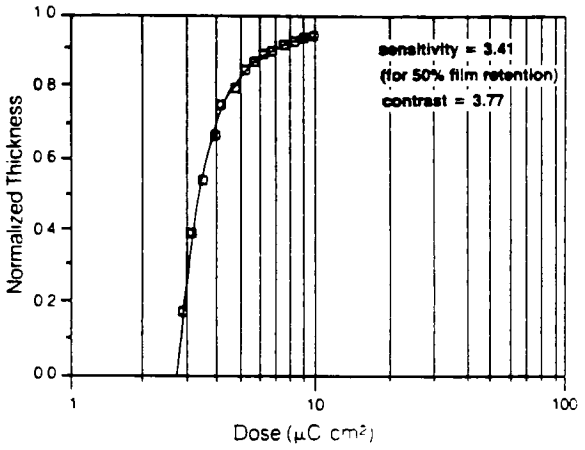
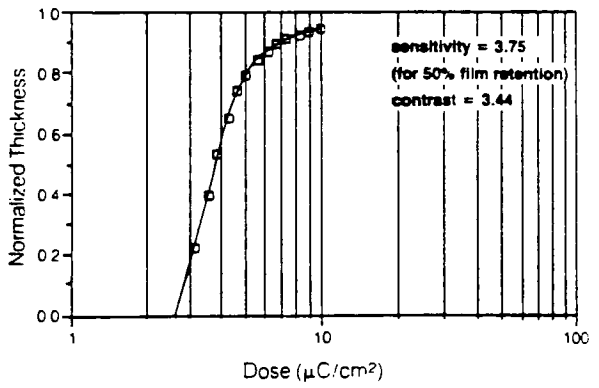


Figure 5

Normalized Thickness vs. Dose
MICROPOSIT SAL660 DEVELOPER
(10 minute immersion)



For Figures 4 and 5
A JEOL JBX-6AII vector-scan variable shaped beam, direct-write machine was used at 20 keV

The use of spray development does not appear to provide better resolution, but may shorten the development cycle. Note that the development time is also a function of the geometries printed. Large unexposed pads will clear rapidly (even as quickly as 45 seconds), but isolated trenches might take much longer to clear.

Long development times will not decrease resis film height in the correctly exposed areas. Electrical linewidth measurements have shown that t change in linewidth per 10% change in development time is less than 5%.

Development of the resist should be done within one day of the post-exposure bake step.

I. Rinse

A deionized water rinse is recommended using a cascade/overflow setup with rinsing continuing until a desired resistivity is reached (example: to an 18 mΩ endpoint).

J. Hardbake (Optional)

Image stability and adhesion is enhanced by an optional hardbake step. Essentially, MICROPOSIT SAL601-ER7 E-BEAM RESIST can be heat treated to withstand high temperatures without flow. For example, a ramped convection bake sequence from 100°C/15 minutes to 190°C/15 minutes in 30°C increments has shown to yield thermal stability to 220°C with no measurable loss of critical dimensions.

Although a deep UV flood is not necessary, MICROPOSIT SAL601-ER7 E-BEAM RESIST can be hardened with a DUV flood exposure step if desired.

K. Etch/Ion Implant

MICROPOSIT SAL601-ER7 E-BEAM RESIST is ideal for use with all common semiconductor wet etchants as well as with plasma and ion implant processes. The dry etch resistance is essentially equivalent to that of the positive resist, MICROPOSIT 2400 PHOTO RESIST, as illustrated in Table I.

Table I

Dry Etching Resistances (Etching Rates In Å/Min)		
SUBSTRATE	SAL601-ER7	SHIPLEY 2400
Nitride	262	251
Oxide	480	424
Al	274	261
Poly-Si	121	162

L. Strip

If MICROPOSIT SAL601-ER7 E-BEAM RESIST has been postbaked below 150°C, it can be stripped with MICROPOSIT 1165 REMOVER. Alternatively, residue free stripping may be accomplished with dry oxygen plasma ashing. Refer to the MICROPOSIT 1165 REMOVER data sheet for the specific processing instructions, specifications, and other product information.

III. Properties As Delivered

MICROPOSIT SAL601-ER7 E-BEAM RESIST is manufactured with advanced manufacturing techniques in state of the art facilities to the highest quality standards and is subjected to state of the art testing for physical, chemical and functional properties to assure the use of maximum lot to lot reproducibility. Each lot is then filtered to 0.2μm absolute directly into precleaned containers with samples being carefully qualified for cleanness Finally, each container is coded with the processing date For additional information, contact your Shipley Technical Sales Representative

A "Quality Statement" can be supplied with each shipment upon request This statement will list the typical quality characteristics of MICROPOSIT SAL601-ER7 E-BEAM RESIST (a Developmental Shipley Advanced Lithography product)

Shown in Table II are the typical properties as delivered

Table II

MICROPOSIT SAL601-ER7 E-BEAM RESIST TYPICAL PROPERTIES	
Solids	~20%
Filterability constant, n/n_0	0.0075 maximum
Water content	0.50% maximum
Index of refraction	1.6 @ 6328 Å
Na, Fe content	<1ppm
Type of solution	solvent base 2-ethoxyethyl acetate n-butyl acetate xylene
Flash point (closed cup)	~41°C
TLV rating	5 ppm

IV. Handling Precautions

WARNING! MICROPOSIT SAL601-ER7 E-BEAM RESIST is a combustible solvent mixture. Vapors are irritating to eyes, nose and respiratory tract. Harmful if swallowed. Do not take internally. Use with adequate ventilation. Avoid breathing vapors Do not get in eyes, on skin or on clothing. Handle with care. Wear chemical goggles, rubber gloves, and protective clothing. Wash thoroughly after handling.

Overexposure to 2-ethoxyethyl acetate has been shown to cause birth defects and adverse effects on pregnancy in laboratory animals.

First Aid:

If swallowed:	Contact a physician at once.
If eye contact:	Flush with water immediately for at least 15 minutes, then contact a physician at once.
If skin contact:	Flush with plenty of water for 15 minutes. Remove contaminated clothing.
If inhaled.	Move into fresh air. Contact physician at once.

For spills, use adequate ventilation. Collect material into a suitable container using absorbent powder.

Consult product Material Safety Data Sheet before using.

V. Equipment

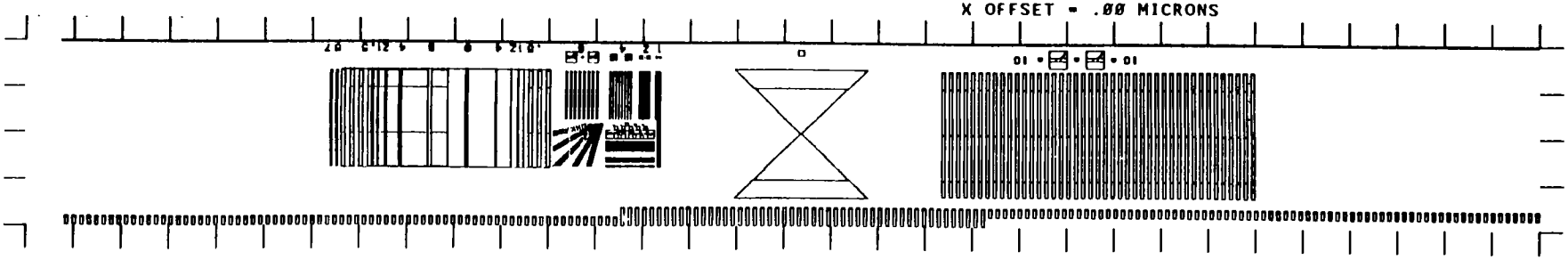
MICROPOSIT SAL601-ER7 E-BEAM RESIST is compatible with most commercially available photoresist processing equipment. Compatible materials include stainless steel, glass, ceramic, unfilled polypropylene, high density polyethylene, polytetrafluoroethylene, or equivalent materials If point of use filtration is used, Teflon[3] filters prewashed with Freon TF are recommended during the coating step For more information, contact your Shipley Technical Sales Representative.

[3]Trademark of E I DuPont de Nemours and Company Inc

Y-AXIS (CM)
0.00
2.00
4.00
6.00
8.00
10.00
X-AXIS (CM)
0.00
2.00
4.00
6.00
8.00
10.00

```
CHECKPAT REV. 4.5          L173634-01-02          5/15/91          MEBES  967
ADDRESS SIZE =    .5000000 MICRONS
DIE DIMENSIONS(X,Y ADDRESSES) =     8000.0000000    1020.0000000
              (X,Y MICRONS   ) =     4000.0000000     510.0000000
NO. OF PASSES =       1 FOR PATTERN MEMORY OF 16384.
NO. OF STRIPES =      4

NUMBER OF RECTAZOIDS =         0.

FIGURE TYPE              NUMBER

RECTANGLES                  757.
PARALLELOGRAMS               30.
LEFT TRAPEZOIDS              11.
RIGHT TRAPEZOIDS             11.
GENERAL TRAPEZOIDS           66.
TOTAL                       875.

AVERAGE TRAPEZOID HEIGHT (ADDRESSES)  47.13
END CHECKPAT FUNCTION
```

```
MEBES  31  PATTERNPLOT REV 7.9 MINICON REV  4.1
PATTERN # = L173634-01-02
DATE PLOTTED 5/15/91  17:27
WINDOW DIMENSION (X/Y,MICRONS) =4000.00/510.00
SCALE = 4 OR 400.00 MICRONS PER INCH
ADDRESS SIZE (MICRONS) = .50
STRIPE HEIGHT (ADDRESSES) = 256
SEGMENT # = 1
PASS # = 1
Y OFFSET = .00 MICRONS
X OFFSET = .00 MICRONS
```



Appendix C - Suprem 4/Medici Sample input decks and plots

```
$ TMA TSUPREM-4 1um PMOS at RIT
$ Date          09/16/91
$ File name     1umpa.in
$ Purpose       'Well creation'
$ Created by    Mark Klare (Masters Thesis Research)
$ This file was made to save simulation time of actual PMOS device
$ by saving the well in a structure file.
$ 1. Identify the graphics driver
OPTION    DEVICE=X
$ 2. Specify the mesh
LINE X     LOCATION=0     SPACING=1.0
LINE X     LOCATION=2.9   SPACING=1.0
LINE X     LOCATION=3.0   SPACING=0.5
LINE X     LOCATION=3.1   SPACING=1.0
LINE X     LOCATION=3.9   SPACING=1.0
LINE X     LOCATION=4.0   SPACING=0.5
LINE X     LOCATION=4.1   SPACING=1.0
LINE X     LOCATION=8.9   SPACING=1.0
LINE X     LOCATION=9.0   SPACING=0.5
LINE X     LOCATION=9.1   SPACING=1.0
LINE X     LOCATION=10    SPACING=0.7
LINE X     LOCATION=10.5  SPACING=0.5
LINE X     LOCATION=11.0  SPACING=0.2
LINE X     LOCATION=11.5  SPACING=0.1
LINE X     LOCATION=11.8  SPACING=0.04
LINE X     LOCATION=12.0  SPACING=0.02
LINE X     LOCATION=12.1  SPACING=0.03
LINE X     LOCATION=12.5  SPACING=0.1
LINE Y     LOCATION=0.0  SPACING=0.01
LINE Y     LOCATION=0.3  SPACING=0.03
LINE Y     LOCATION=1.0  SPACING=0.08
LINE Y     LOCATION=2    SPACING=0.3
LINE Y     LOCATION=6    SPACING=1.0
ELIMINATE  COLUMNS  Y.MIN=0.8   X.MIN=11.9  X.MAX=12.1
ELIMINATE  COLUMNS  Y.MIN=2.0
ELIMINATE  COLUMNS  Y.MIN=2.5
ELIMINATE  COLUMNS  Y.MIN=3.0
$ 3. Initialize
INITIALIZE <100>  Phosphor=1E15
$ 4. Plot the initial mesh
$ option     Plot.out=mesh.plt
SELECT     TITLE="Initial Mesh"
PLOT.2D   Y.MAX=3.0 SCALE X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0
 T.SIZE=0.4 L.BOUND=1 C.BOUND=1 GRID L.GRID=1 C.GRID=1
$ 5. Initial oxide pad
Diffuse time=8 temperat=1100 dryo2
$ 6. Use the VERTICAL method for oxidation
METHOD     VERTICAL  GRID.OXI=4
$ 7. Print oxide thickness
Select  Z=1   Title="Pad oxide"
Print.1d layers x.v=5.0
$ 8. Mass implant to change surface
IMPLANT    phosphor  DOSE=5.0E12  ENERGY=50
$ 9. Etch pad before field growth
Etch oxide all
```

```
$ 10. Field oxide growth
```



```
DIFFUSE    TEMP=1100  TIME=150  DRYO2
$ 11. Substrate doping profile
$ Option           plot.out=doping.plt
SELECT     Z=LOG10(phosphor)  TITLE="Channel Doping after field"
PLOT.1D    X.VALUE=5.0  X.MAX=3.0  LINE.TYP=2  Y.MIN=15 Y.MAX=19
LABEL      X=1.8 Y=18.5  LABEL="Phosporous" LINE=2
$ 12. Print oxide thickness
Select  Z=1   Title="Field oxide"
Print.1d layers x.v=5.0
$ 13. Etch oxide
Etch    Oxide all
$ 14. Save as structure file for future tests
STRUCTURE  OUTFILE=1umpa.str
$ 15. End of input file
STOP
```

```
$ SUPREM4 1um PMOS Mark Klarre
$ Date          09/16/91
$ File name     1ump.in
$ Created by    Mark Klare (Masters Thesis Research)
$ Steps 1-15 are contained in a structure file called 1umpa.str
$ .75um devise with 2um shallow drain width on either side of S/D.
$ 1. Identify the graphics driver
OPTION    DEVICE=X
$ 2. Load in 'well' structure file
initialize   infile=1umpa.str
$ 2.2 deposit photoresist
DEPOSITION PHOTORES POSITIVE THICKNES=0.8 SPACES=1
$ 2.3 etch resist
ETCH      PHOTORES START X=3.125 Y=-2.0
ETCH      CONTINUE X=10.125 Y=-2.0
ETCH      CONTINUE X=10.125 Y=2.0
ETCH      PHOTORES DONE X=3.125 Y=2.0
$ 2.5 contact implant
Implant    boron energy=100 dose=1.0e15
$ 2.7  etch remaining resist
Etch       photores all
$ 3. Gate oxidation
DIFFUSE    TEMP=950  TIME=60  DRYO2
$ 4. Print oxide and silicon thicknesses
SELECT     Z=0
PRINT.1D   X.VALUE=5.0  LAYERS
$ 5. Poly deposition
DEPOSIT    POLYSILICON  THICKNESS=0.3  DIVISIONS=4
$ 5.5 Poly doping implant
Implant    boron energy=45 dose=1e15
$ 6. Poly etch between x = 0.0 and 12.0 microns
ETCH      POLYSILI LEFT P1.X=12.125
$ 6.5 Mask for D/S Implant
DEPOSIT    Photores  THICK=1.2  SPACES=3
ETCH       Photores  right p1.x=3.0
$ 7. Drain/Source Implants
IMPLANT    boron  ENERGY=60  DOSE=5E15 name=bf2
$ 7.5 etch resist
etch       photores all
$ 8. Doping profile
$ Option     Plot.out=dsimp.plt
SELECT     Z=LOG10(Phosphor) Title="D/S IMP  (D/S)" label="Log (Concentration)"
PLOT.1D    X.VALUE=10.5  x.max=3 line.typ=1 y.min=15 y.max=19
Label      x=2.0 y=18 label="Phosphorous" line=1
SELECT     Z=Log10(Boron)
PLOT.1D    X.V=10.5 ^axes ^clear line.typ=2
Label      x=2.0 y=17.6 label="Boron" line=2
SELECT     Z=Log10(doping)
PLOT.1D    X.V=10.5 ^axes ^clear line.typ=3
Label      x=2.0 y=17.2 label="Net doping" line=3
$ 8. Doping profile
$ Option     Plot.out=dsimpc.plt
SELECT     Z=LOG10(Phosphor) Title="D/S IMP  (CHANNEL)" label="Log (Concentratio
PLOT.1D    X.VALUE=12.5  x.max=3 line.typ=1 y.min=15 y.max=19
Label      x=2.0 y=18 label="Phosphorous" line=1
```

```
SELECT     Z=Log10(Boron)
```



```
PLOT.1D    X.V=12.5 ^axes ^clear line.typ=2
Label      x=2.0 y=17.6 label="Boron" line=2
SELECT     Z=Log10(doping)
PLOT.1D    X.V=12.5 ^axes ^clear line.typ=3
Label      x=2.0 y=17.2 label="Net doping" line=3
$ 23. Grow oxide for contact cuts and activate S/D
diffuse    temp=850 time=40 dryo2
$ 8. Doping profile
$ Option     Plot.out=lastdop.plt
SELECT     Z=LOG10(Phosphor) Title="Doping Profile after Activation" label="Log
PLOT.1D    X.VALUE=10.0  x.max=3 line.typ=1 y.min=15 y.max=19
Label      x=2.0 y=18 label="Phosphorous" line=1
SELECT     Z=Log10(Boron)
PLOT.1D    X.V=10.0 ^axes ^clear line.typ=2
Label      x=2.0 y=17.6 label="Boron" line=2
SELECT     Z=Log10(doping)
PLOT.1D    X.V=10.0 ^axes ^clear line.typ=3
Label      x=2.0 y=17.2 label="Net Doping" line=3
$ 8. Doping profile
$ Option     Plot.out=lastdopc.plt
SELECT     Z=LOG10(Phosphor) Title="Doping Profile after Activation" label="Log
PLOT.1D    X.VALUE=12.5 x.max=3 line.typ=1 y.min=15 y.max=19
Label      x=2.0 y=18 label="Phosphorous" line=1
SELECT     Z=Log10(Boron)
PLOT.1D    X.V=12.5 ^axes ^clear line.typ=2
Label      x=2.0 y=17.6 label="Boron" line=2
SELECT     Z=Log10(doping)
PLOT.1D    X.V=12.5 ^axes ^clear line.typ=3
Label      x=2.0 y=17.2 label="Net Doping" line=3
$ 18. Print oxide and silicon thicknesses
SELECT     Z=1
PRINT.1D   X.VALUE=0.0  LAYERS
$ 22. Etch contact cuts
ETCH      OXIDE START X=4.125 Y=-.5
ETCH      CONTINUE X=9.125 Y=-.5
ETCH      CONTINUE X=9.125 Y=.5
ETCH      DONE X=4.125 Y=.5
$ 23. Metallization / Etch for contacts
DEPOSIT    ALUMINUM  THICK=0.5  SPACES=3
ETCH      ALUMINUM RIGHT P1.X=10.125
$ 24. Reflect to form the complete structure; then save it
STRUCTURE  OUTFILE=1ump.str
STRUCTURE  REFLECT  RIGHT
STRUCTURE OUT.FILE=1umpt.pis SCALE=1.0 MEDICI POLY.ELE
$ 25. End of input file
STOP
```

```
TITLE   1um PMOS simulation
$ 1. Read in the Mesh file taken from 1ump.in
MESH       TSUPREM4 IN.FILE=1umpt.pis RECTANGU
$ 2. Solve for holes using a Newtonian solution
SYMBOLIC   NEWTON CARRIERS=1 HOLES PRINT
$ 3. Save the I-V characteristic data in a file
LOG        IVFILE=1.iv
$ 4. Obtain a solution with variable gate voltage
SOLVE      V1=0.0 V2=0.0 V3=-0.1 ELECTROD=(1) VSTEP=-0.5 NSTEPS=8 +
 OUT.FILE=zero.out ASCII
```

```
Title   1um PMOS simulation

$ 1. Read in the Mesh file taken from 1ump.in
Mesh    Infile=1umpt.pis tsuprem4

$ 2. Solve for holes using a Newtonian solution
Symbol  holes print newton carriers=1

$ 3. Save the I-V characteristic data in a file
Log     ivfile=2.iv gate=1 source=2 drain=3 substrate=4

$ 4. Obtain a solution with variable gate voltage
SOLVE     V1=0.0 V2=0.0 V3=-5.0 ELECTROD=(1) VSTEP=-0.5 NSTEPS=8 +
 OUT.FILE=five.out
```

```
$ Suprem 4 input deck to plot output of 1ump.in
$ Identify the graphics driver
 OPTION    DEVICE=x
$ Read the structure
INITIALIZE INFILE=1ump.str
STRUCTURE  REFLECT RIGHT
$ Prepare to plot contours of boron, phosphorous, and arsenic
SELECT     TITLE="PMOS Cross Section"
PLOT.2D    SCALE  Y.max=2.0 y.min=-0.5 x.max=12.5 x.min=1.0
SELECT     Z=LOG10(Boron)
FOREACH    VAL (14 TO 21 STEP 1)
  CONTOUR    VALUE=VAL  LINE=4
END
SELECT     Z=LOG10(Phosphorus)
FOREACH    VAL (14 TO 21 STEP 1)
  CONTOUR    VALUE=VAL  LINE=6
END
$ Add labels
$LABEL      X=0.01  Y=-0.8    LABEL="Aluminum"
$LABEL      X=1.99  Y=-0.8    LABEL="Aluminum"  RIGHT
$LABEL      X=1.0   Y=-0.2    LABEL="Poly"      CENTER
$LABEL      X=0.05  Y=0.35    LABEL="Source"
$LABEL      X=1.95  Y=0.35    LABEL="Drain"     RIGHT
$ Plot the grid
$ OPTION     PLOT.OUT=FMESH.PLT
SELECT     TITLE="Final Mesh"
PLOT.2D    GRID  SCALE  Y.MAX=3
STOP
```

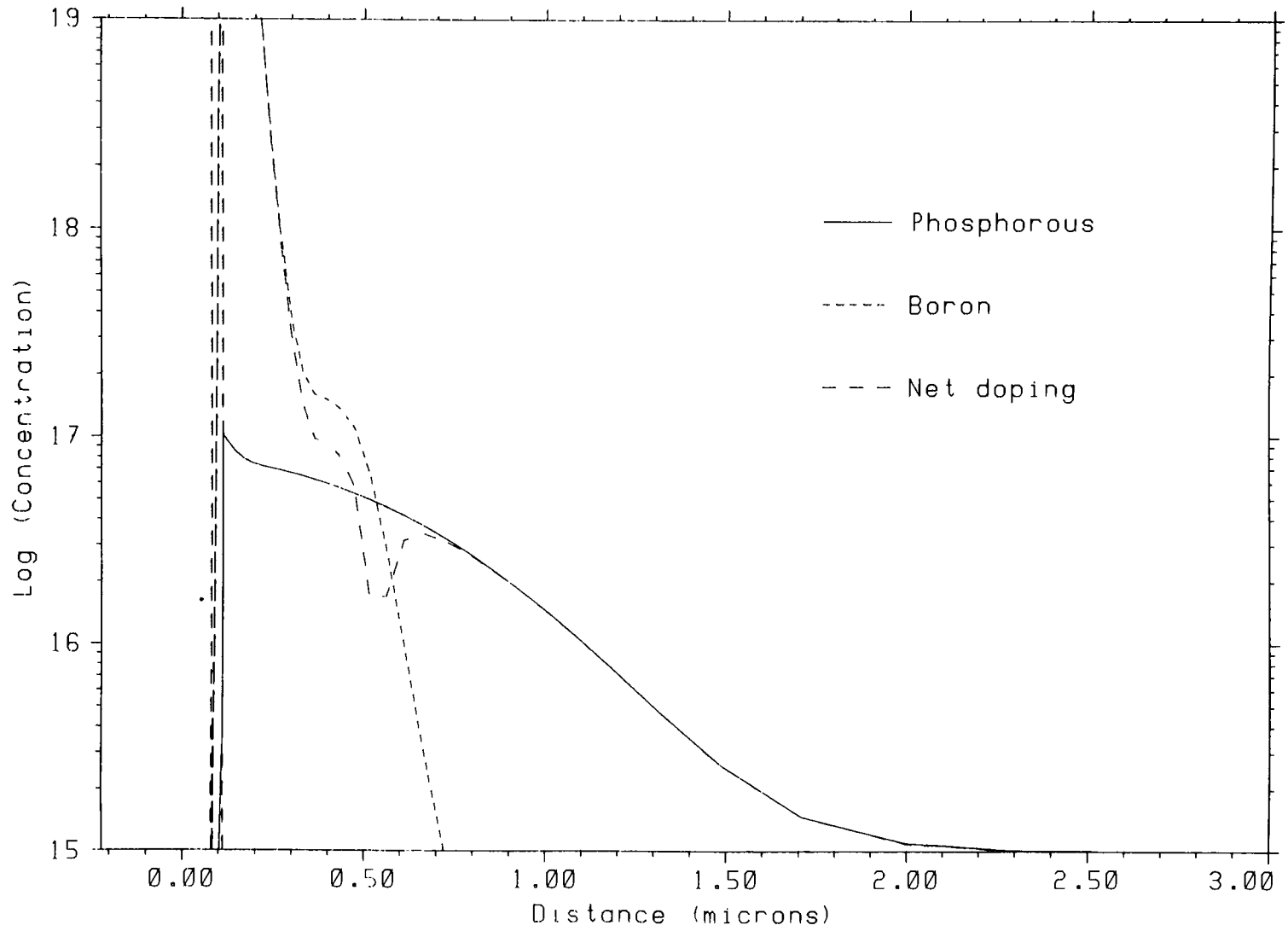
```
TITLE   Hole concentration
$ 1. Read in the mesh generated from lump.in
MESH      TSUPREM4 IN.FILE=lumpt.pis RECTANGU
$ 2. Read in solution from pisces.in
LOAD      ^ASCII.IN IN.FILE=five.ovb
$ 3. Plot a small cross section of the device
PLOT.2D   BOUNDARY JUNCTION DEPLETIO FILL X.MIN=0 X.MAX=25 Y.MAX=1.5 +
 X.OFFSET=2.0 Y.OFFSET=2.0 TITLE="Hole concentration." T.SIZE=0.4 SCALE +
 X.SIZE=0.25 Y.SIZE=0.25 TIMESTAM TIME.SIZ=0.25 DEVICE=x
$ 4. Place the potential contours on the graph depl.plt
CONTOUR   HOLES ABSOLUTE FILL C.START=8 C.INCREM=1 LINE.TYP=1 COLOR=1
```

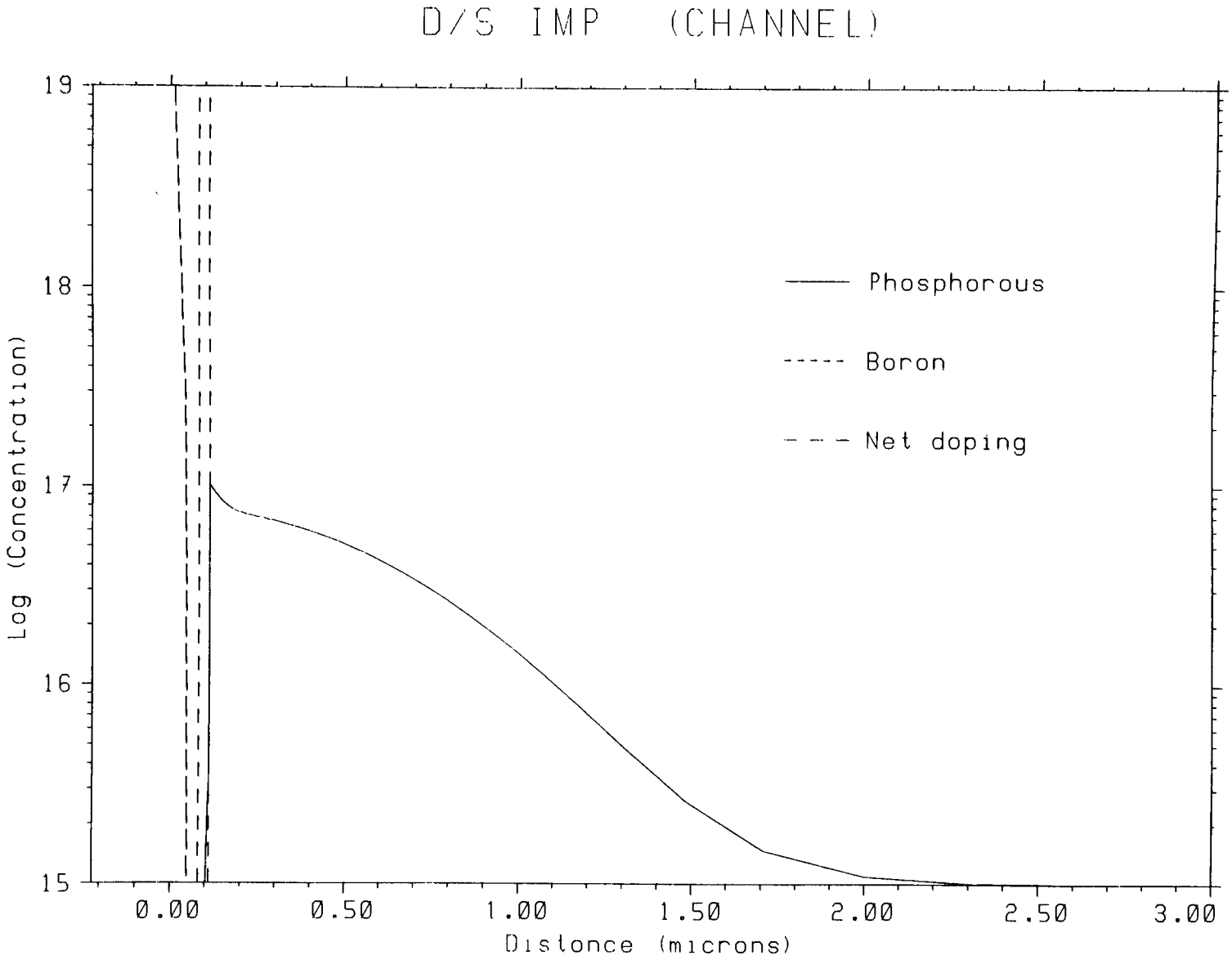
```
TITLE  PMOS Cross Section  Gate=4.0v Drain=-5.0v
$ 1. Read in the mesh generated from 1ump.in
MESH      TSUPREM4 IN.FILE=1umpt.pis RECTANGU
$ 2. Read in solution from pisces.in
LOAD      ^ASCII.IN IN.FILE=five.out
$ 3. Plot the cross section of the device
PLOT.2D   BOUNDARY JUNCTION DEPLETIO X.MIN=10.0 X.MAX=15.0 Y.MAX=1.5 +
 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 SCALE X.SIZE=0.25 Y.SIZE=0.25 DEVICE=x
$ 4. Place the potential contours on the graph
CONTOUR   POTENTIA MIN.VALU=-5.0 MAX.VALU=0.0 DEL.VALU=1.0 FILL C.START=8 +
 C.INCREM=1 LINE.TYP=1 COLOR=1
```

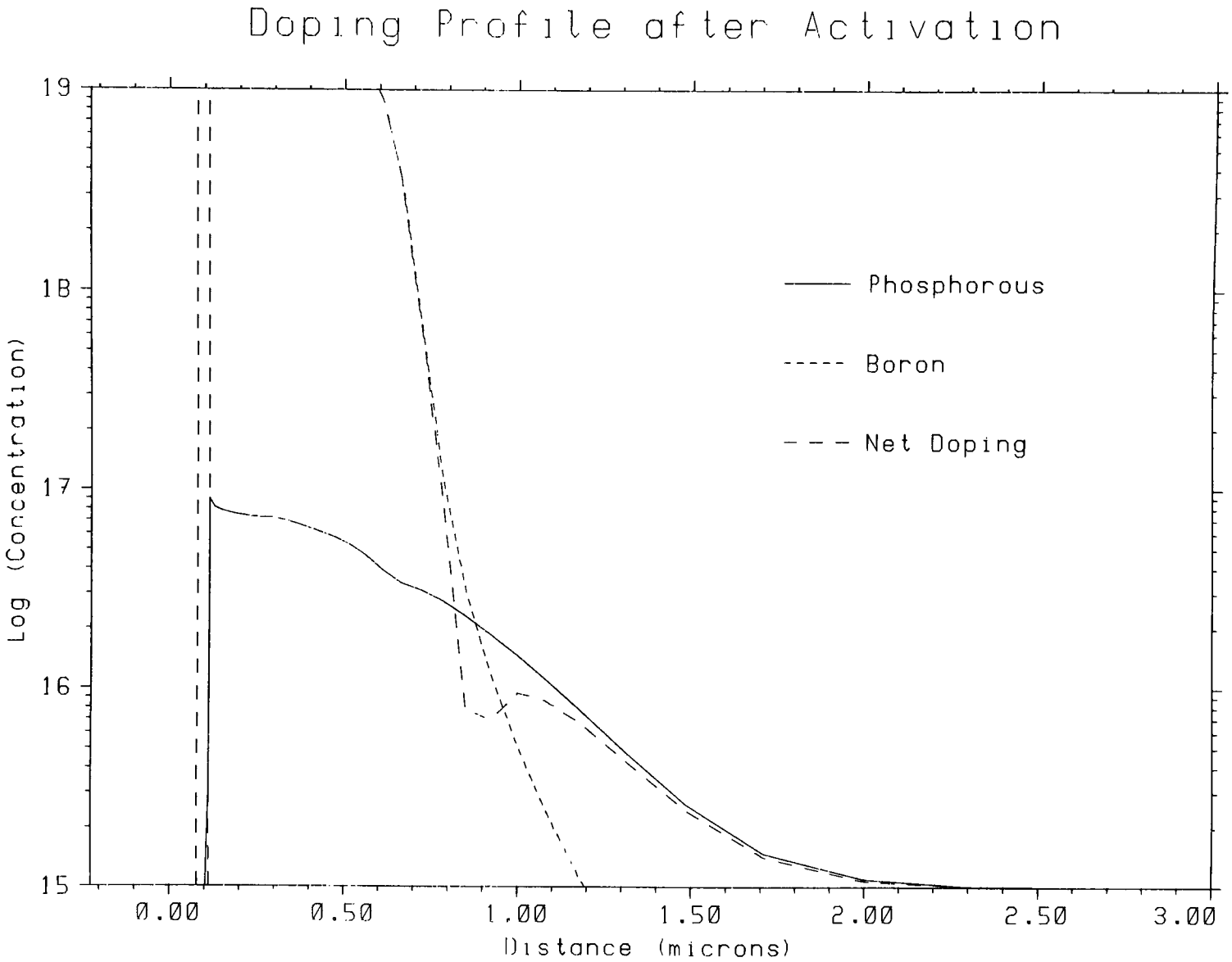
```
Title   Field lines
$ 1. Read in the mesh generated from 1ump.in
MESH      TSUPREM4 IN.FILE=1umpt.pis RECTANGU
$ 2. Read in solution from pisces.in
LOAD      ^ASCII.IN IN.FILE=five.ovb
$ 3. Plot a small cross section of the device
PLOT.2D   BOUNDARY JUNCTION DEPLETIO X.MIN=9 X.MAX=16 Y.MAX=1.0 X.OFFSET=2.0 +
 Y.OFFSET=2.0 T.SIZE=0.4 SCALE X.SIZE=0.25 Y.SIZE=0.25 DEVICE=x
$ 4. Place the hole conc. contours on the graph holes.plt
CONTOUR   POTENTIA FILL C.START=8 C.INCREM=1 LINE.TYP=1 COLOR=1
```

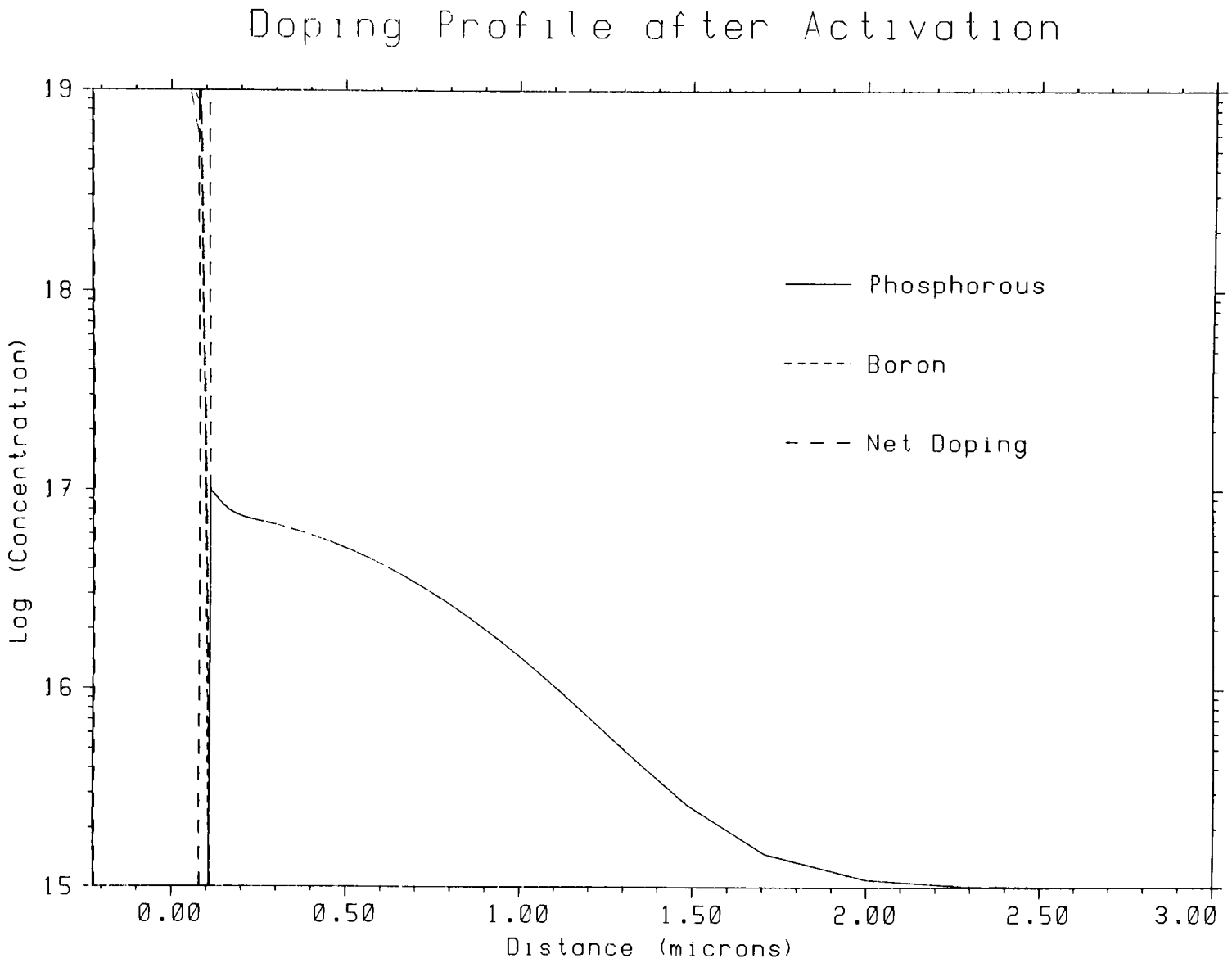
```
Title   Hole concentration
$ 1. Read in the mesh generated from 1ump.in
Mesh    infile=1umpt.pis  tsuprem4
$ 2. Read in solution from pisces.in
LOAD      ^ASCII.IN IN.FILE=five.ovb
$ 3. Plot a small cross section of the device
PLOT.2D   BOUNDARY JUNCTION DEPLETIO X.MIN=9 X.MAX=16 Y.MAX=2 X.OFFSET=2.0 +
 Y.OFFSET=2.0 T.SIZE=0.4 SCALE X.SIZE=0.25 Y.SIZE=0.25 DEVICE=x
$ 4. Place the hole conc. contours on the graph holes.plt
CONTOUR   HOLES ABSOLUTE LOGARITH MIN.VALU=14 MAX.VALU=18 NCONTOUR=5 FILL +
 C.START=8 C.INCREM=1 LINE.TYP=1 COLOR=1
```

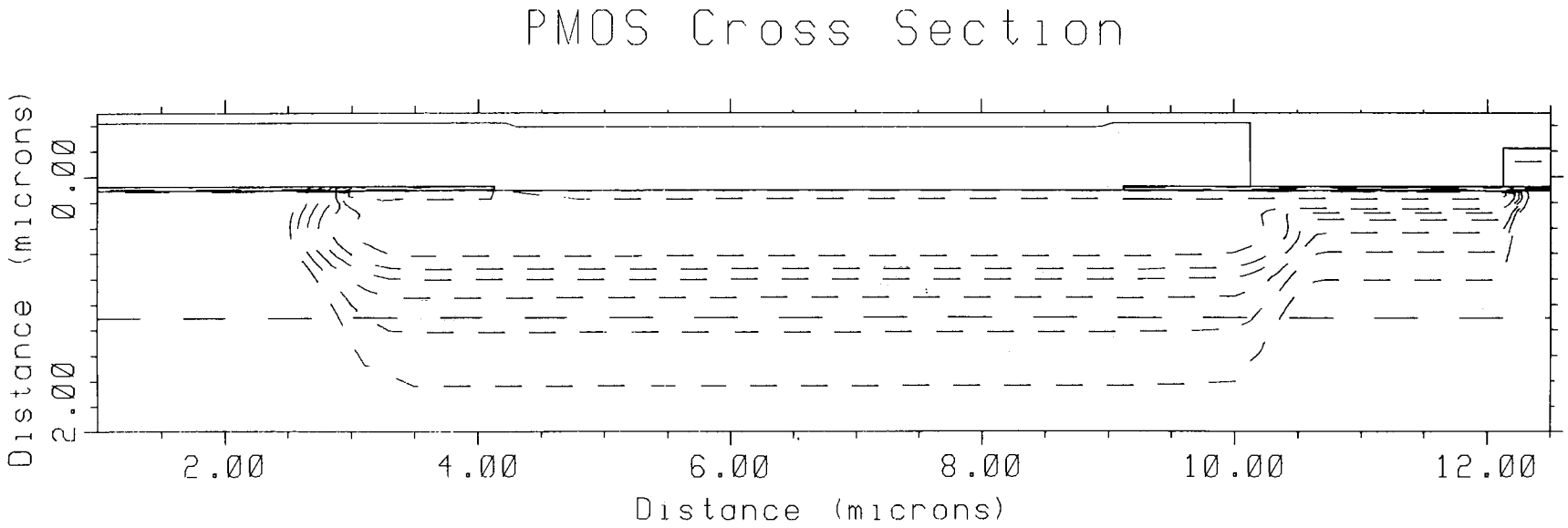
```
Title   Threshold Voltage (.1 volt drain)
PLOT.1D   X.AXIS=v1 Y.AXIS=I2 IN.FILE=2.iv T.SIZE=0.4 X.SIZE=0.25 Y.SIZE=0.25 +
 POINTS C.SIZE=0.25 LINE.TYP=1 COLOR=1 DEVICE=x
```

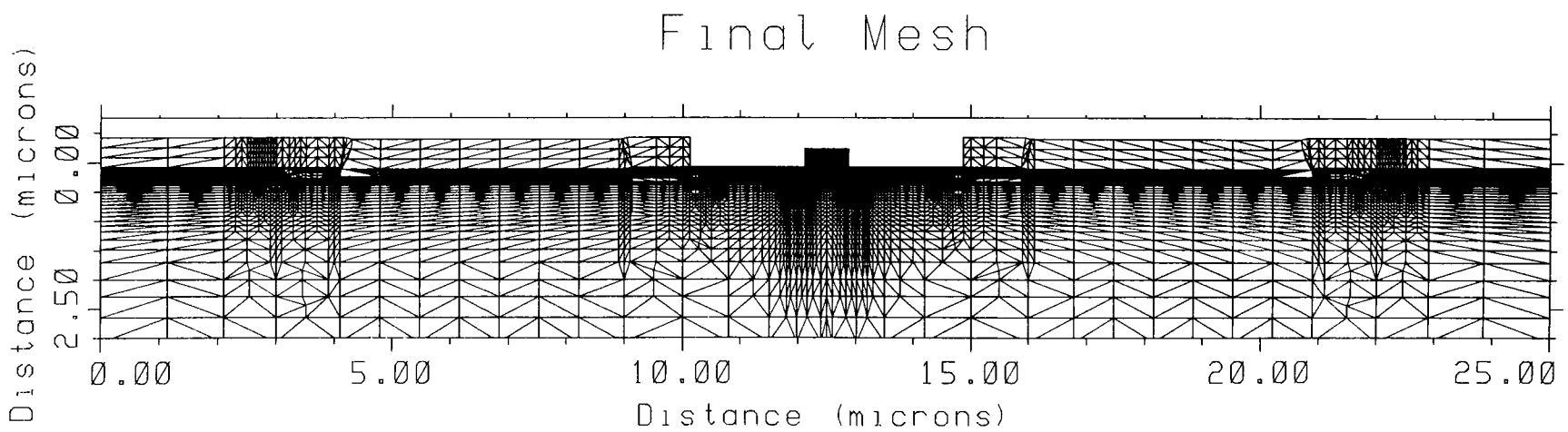

D/S IMP (D/S)
19
18
17
16
15
Log (Concentration)
0.00
0.50
1.00
1.50
2.00
2.50
3.00
Distance (microns)
Phosphorous
Boron
Net doping

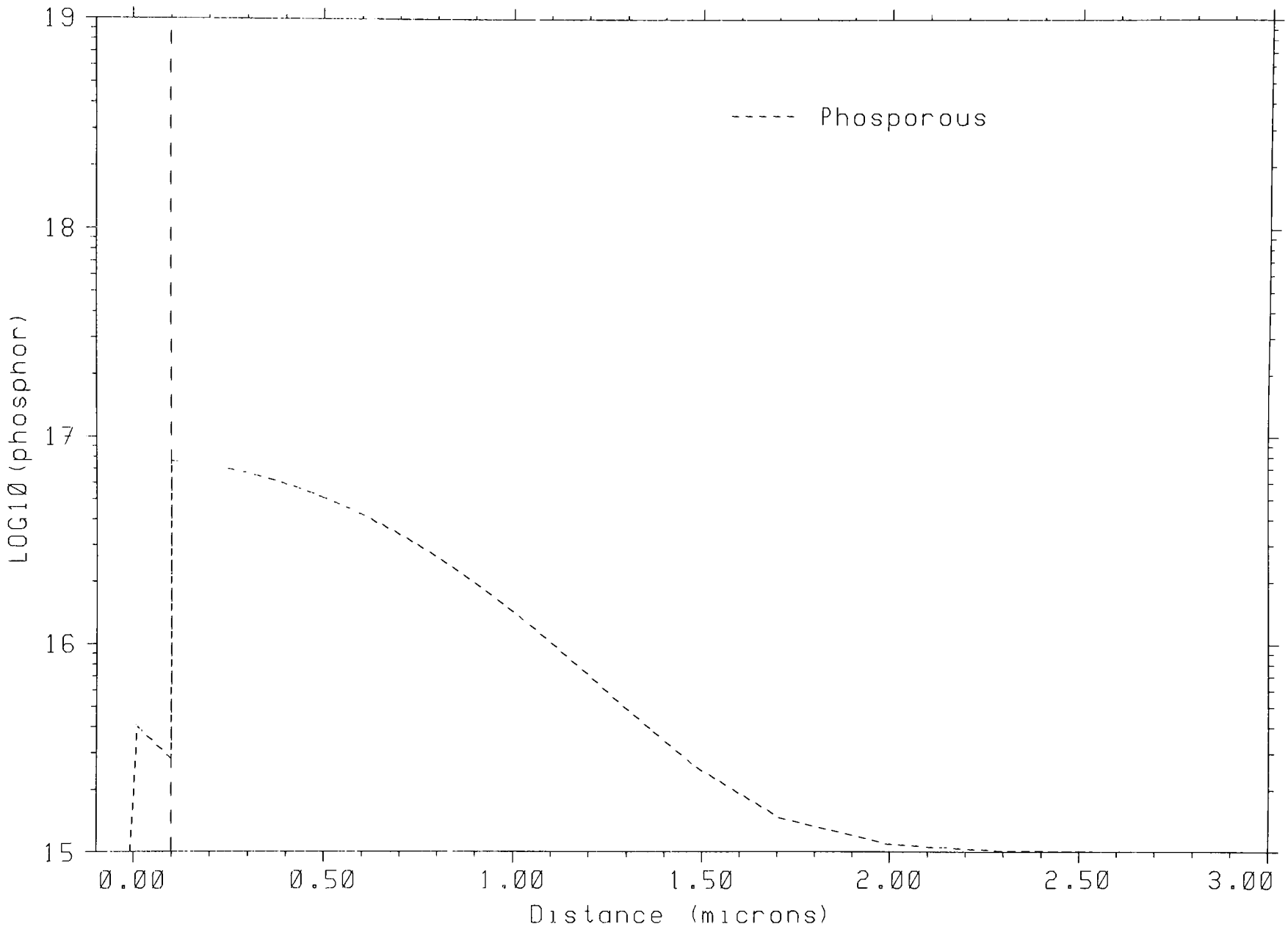

D/S IMP (CHANNEL)
19
18
17
16
15
Log (Concentration)
0.00
0.50
1.00
1.50
2.00
2.50
3.00
Distonce (microns)
Phosphorous
Boron
Net doping

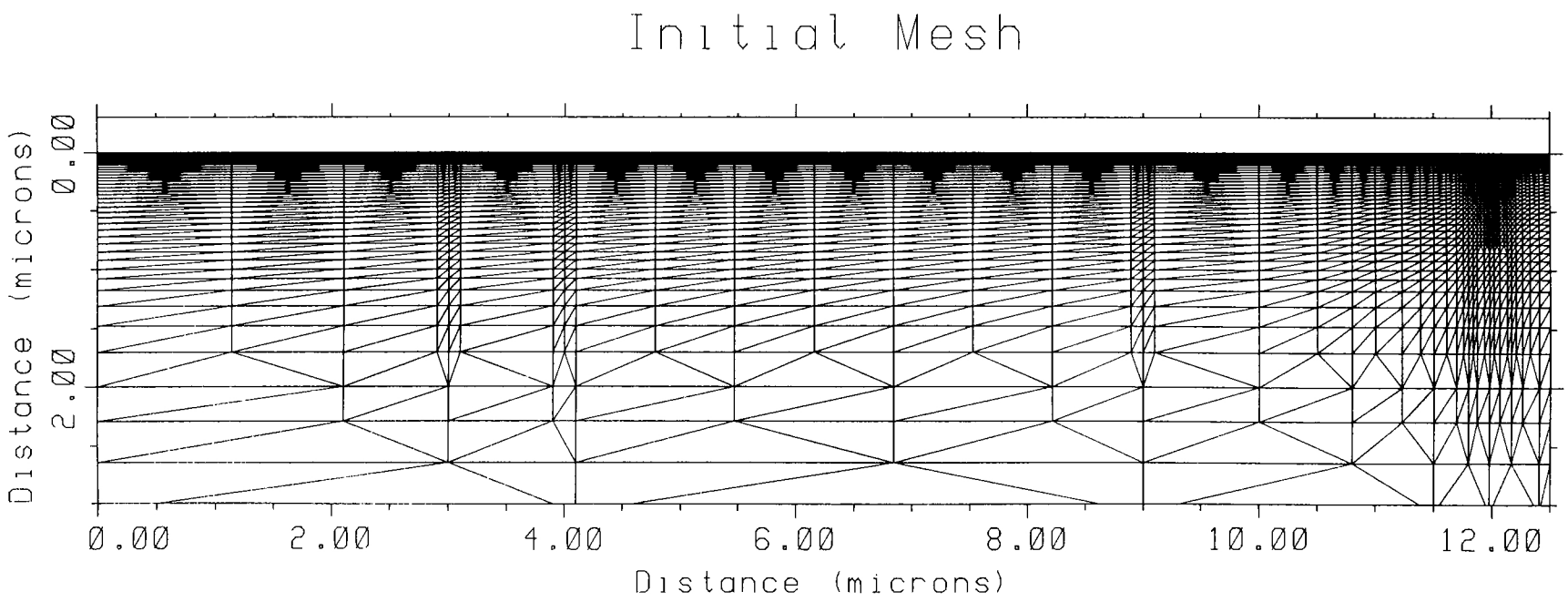

Doping Profile after Activation
19
18
17
16
15
Log (Concentration)
0.00
0.50
1.00
1.50
2.00
2.50
3.00
Distance (microns)
Phosphorous
Boron
Net Doping

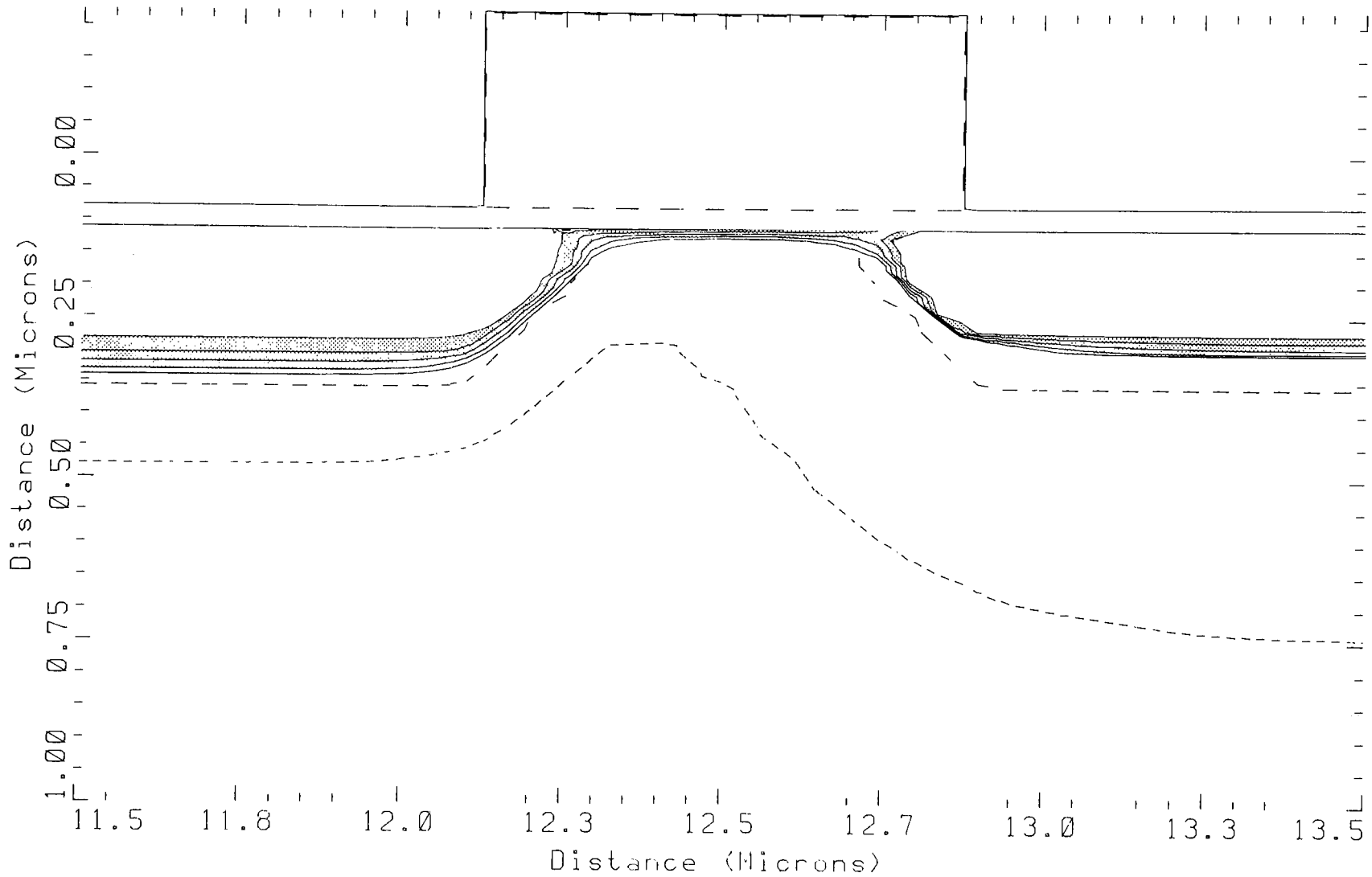

Doping Profile after Activation
19
18
17
16
15
Log (Concentration)
0.00
0.50
1.00
1.50
2.00
2.50
3.00
Distance (microns)
Phosphorous
Boron
Net Doping

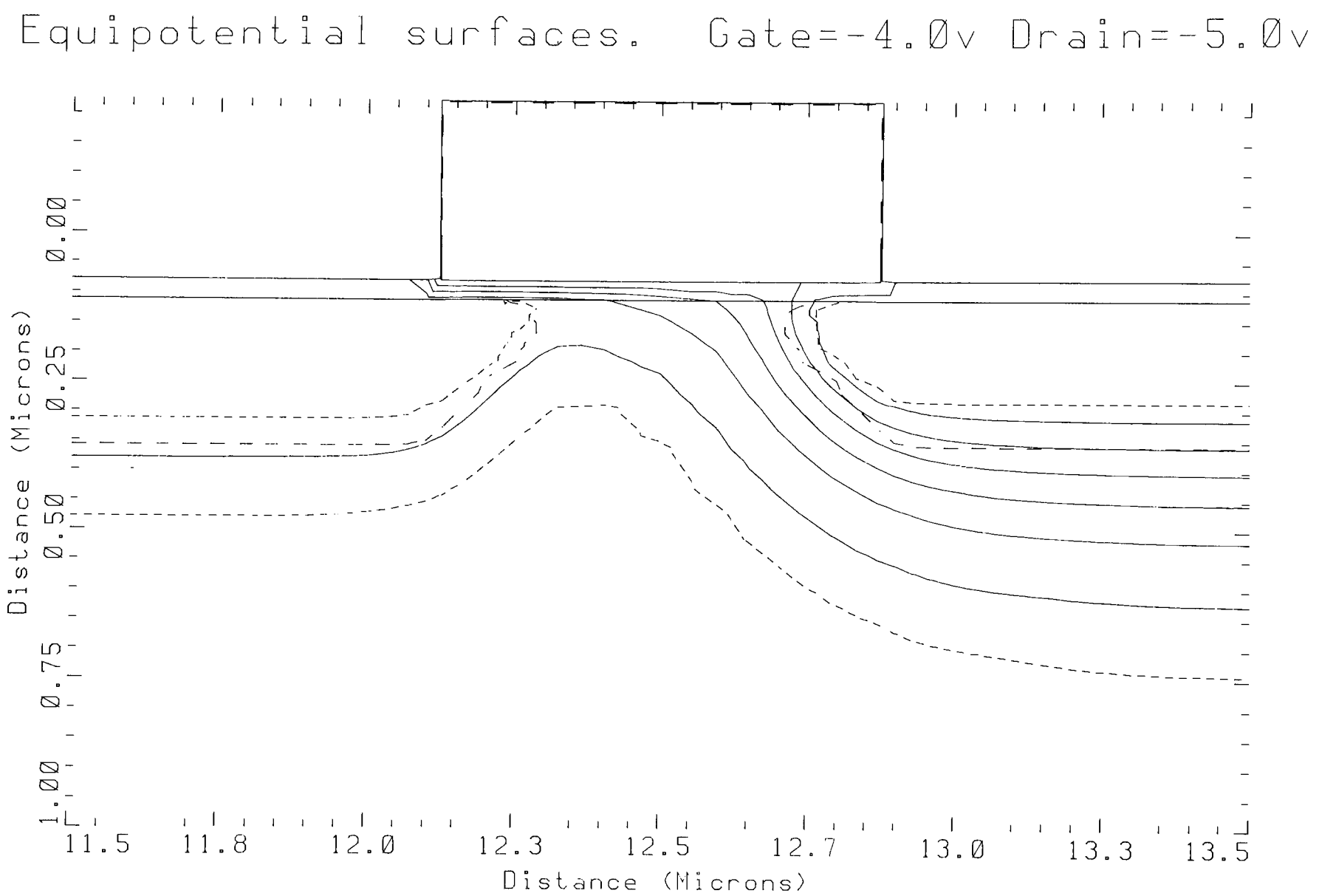

PMOS Cross Section
Distance (microns)
0.00
2.00
2.00
4.00
6.00
8.00
10.00
12.00
Distance (microns)

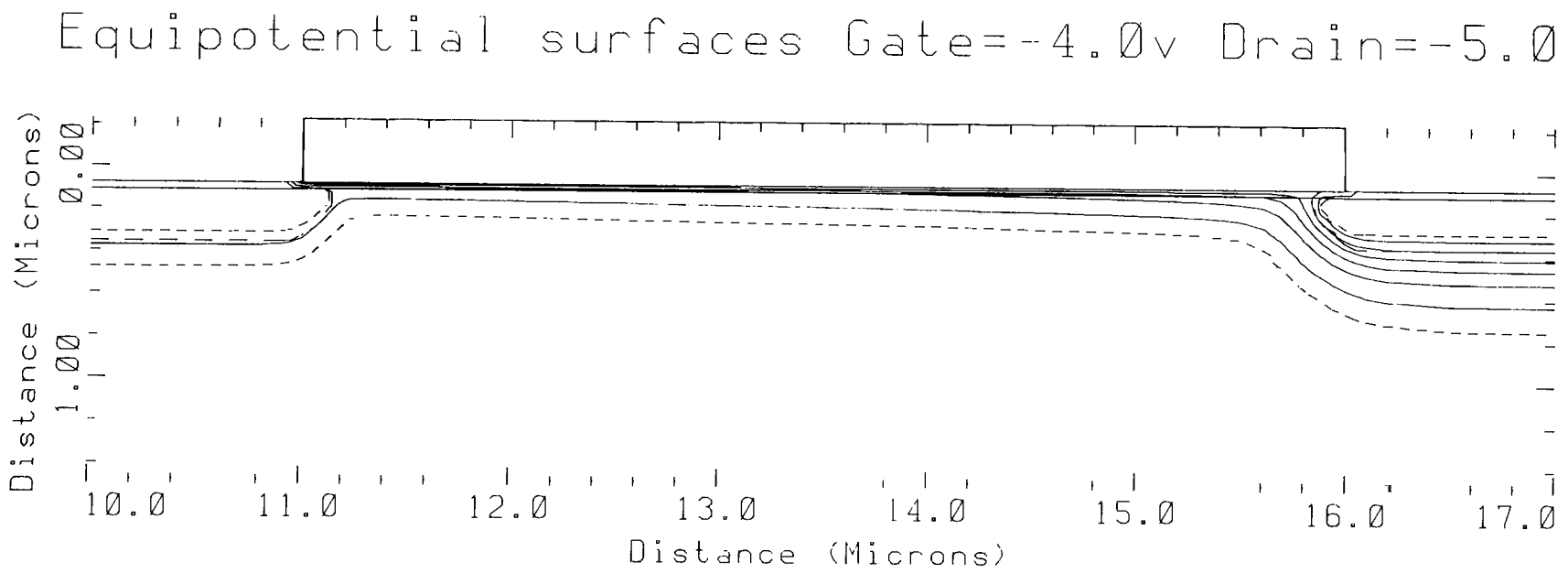

Final Mesh
Distance (microns)
0.00
2.50
0.00
5.00
10.00
15.00
20.00
25.00
Distance (microns)

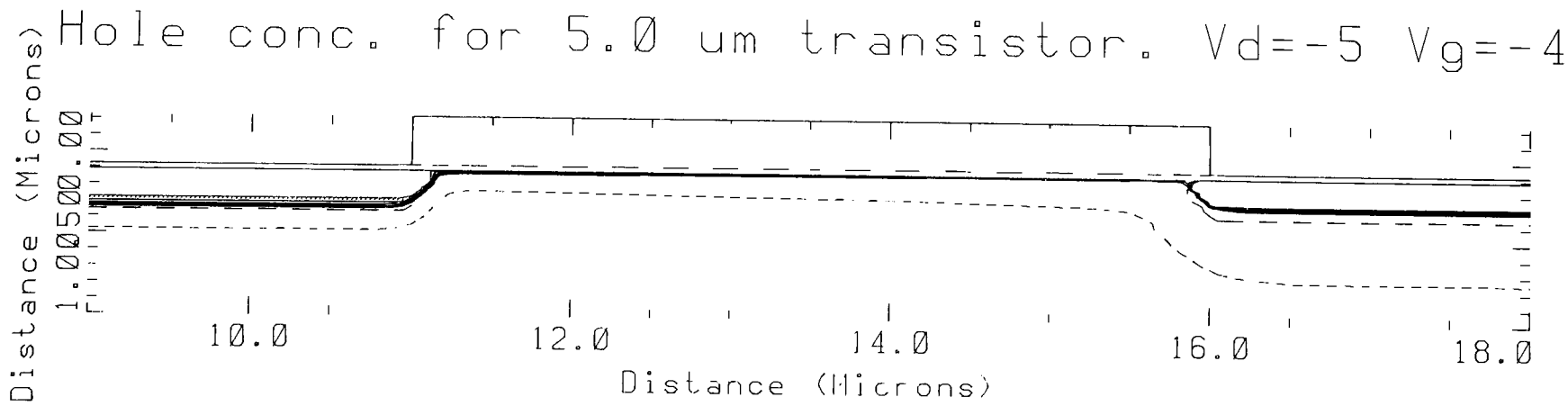

Channel Doping after field
19
18
17
16
15
LOG10(phosphor)
----- Phosporous
0.00
0.50
1.00
1.50
2.00
2.50
3.00
Distance (microns)


Initial Mesh
Distance (microns)
0.00
2.00
0.00
2.00
4.00
6.00
8.00
10.00
12.00
Distance (microns)

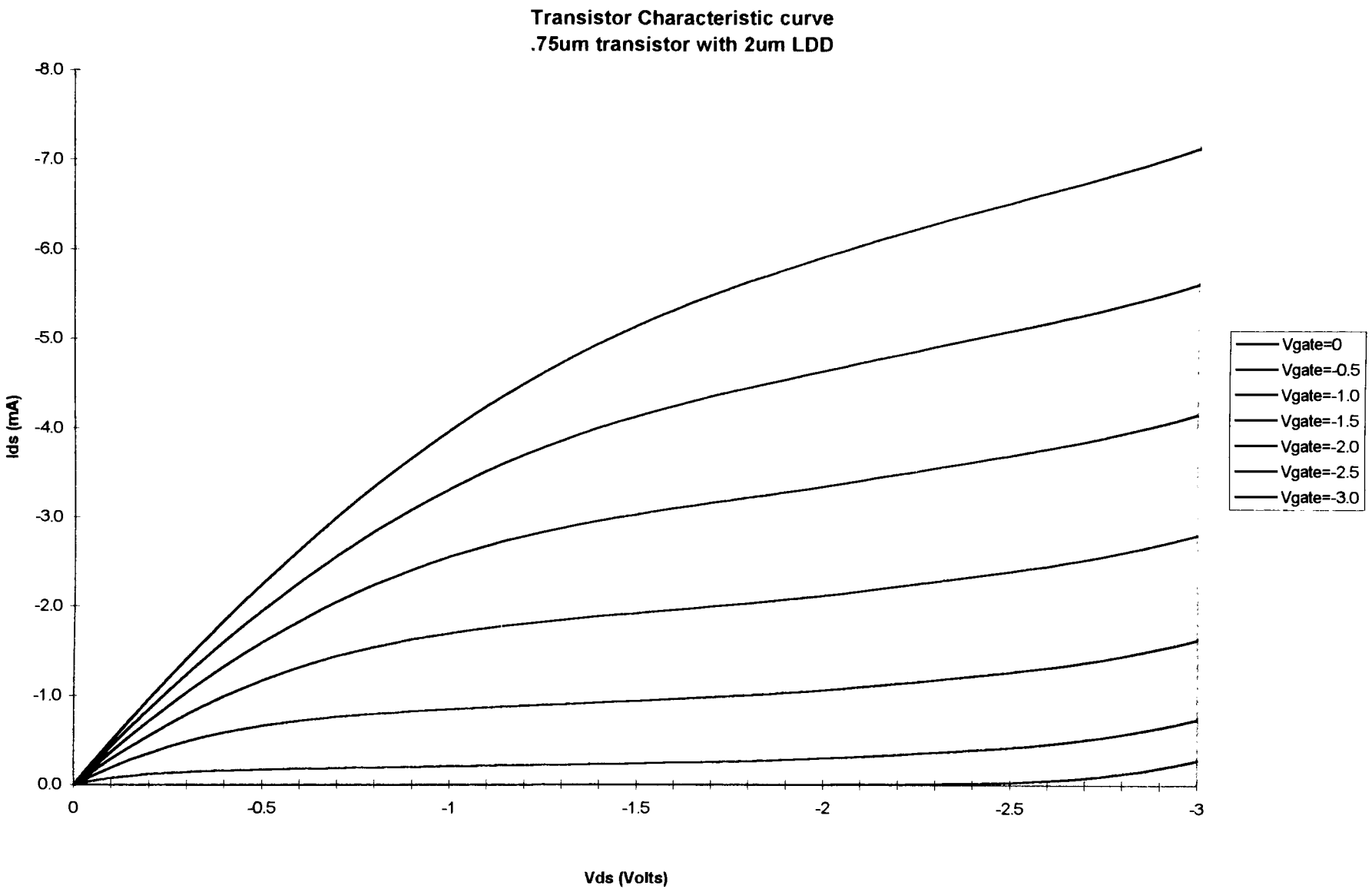

Hole conc. for 0.75 um transistor. Vd=-5 Vg=-4
0.00
0.25
0.50
0.75
1.00
Distance (Microns)
11.5
11.8
12.0
12.3
12.5
12.7
13.0
13.3
13.5
Distance (Microns)

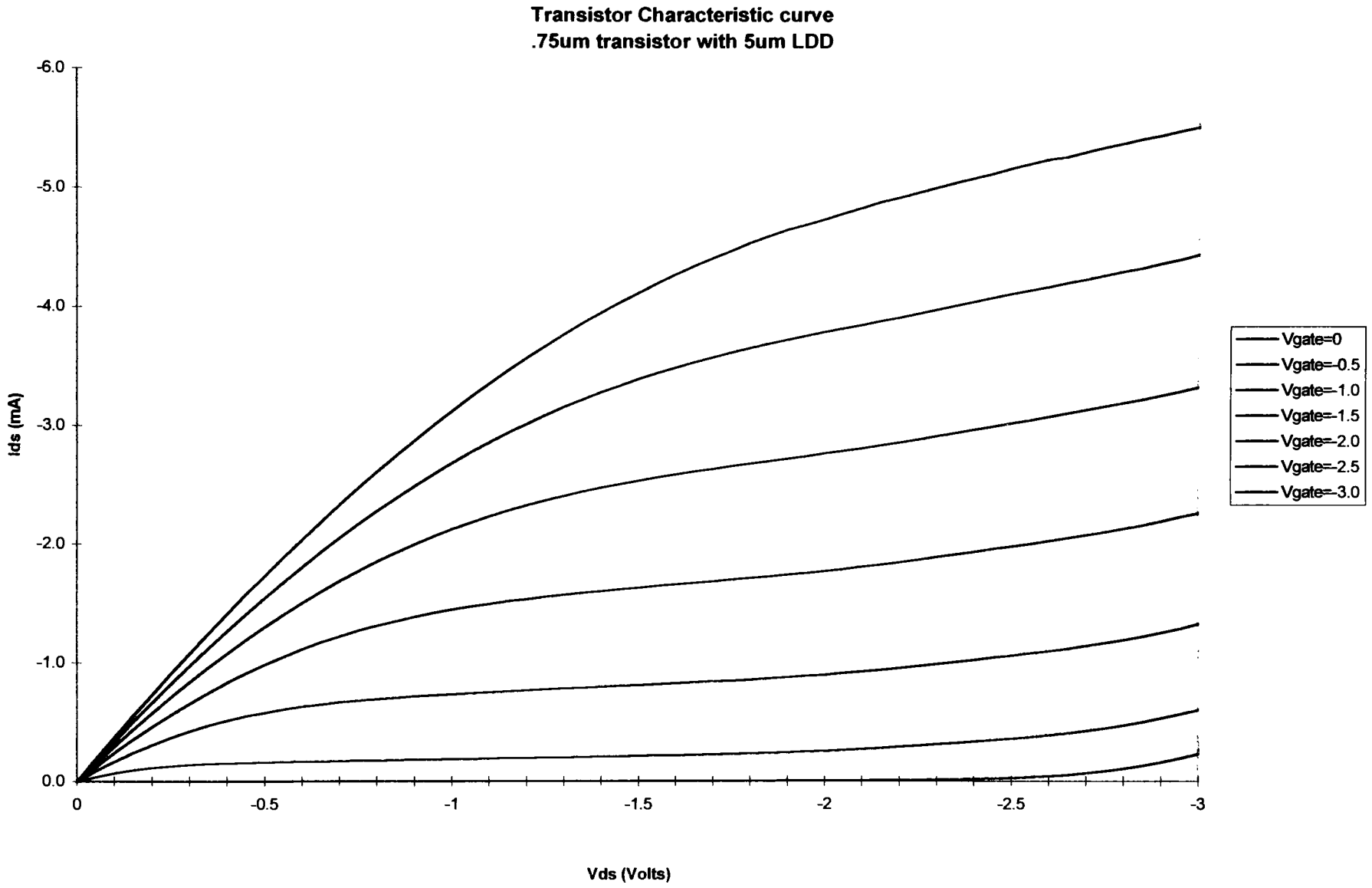

Equipotential surfaces. Gate=-4.0v Drain=-5.0v
0.00
0.25
0.50
0.75
1.00
Distance (Microns)
11.5
11.8
12.0
12.3
12.5
12.7
13.0
13.3
13.5
Distance (Microns)

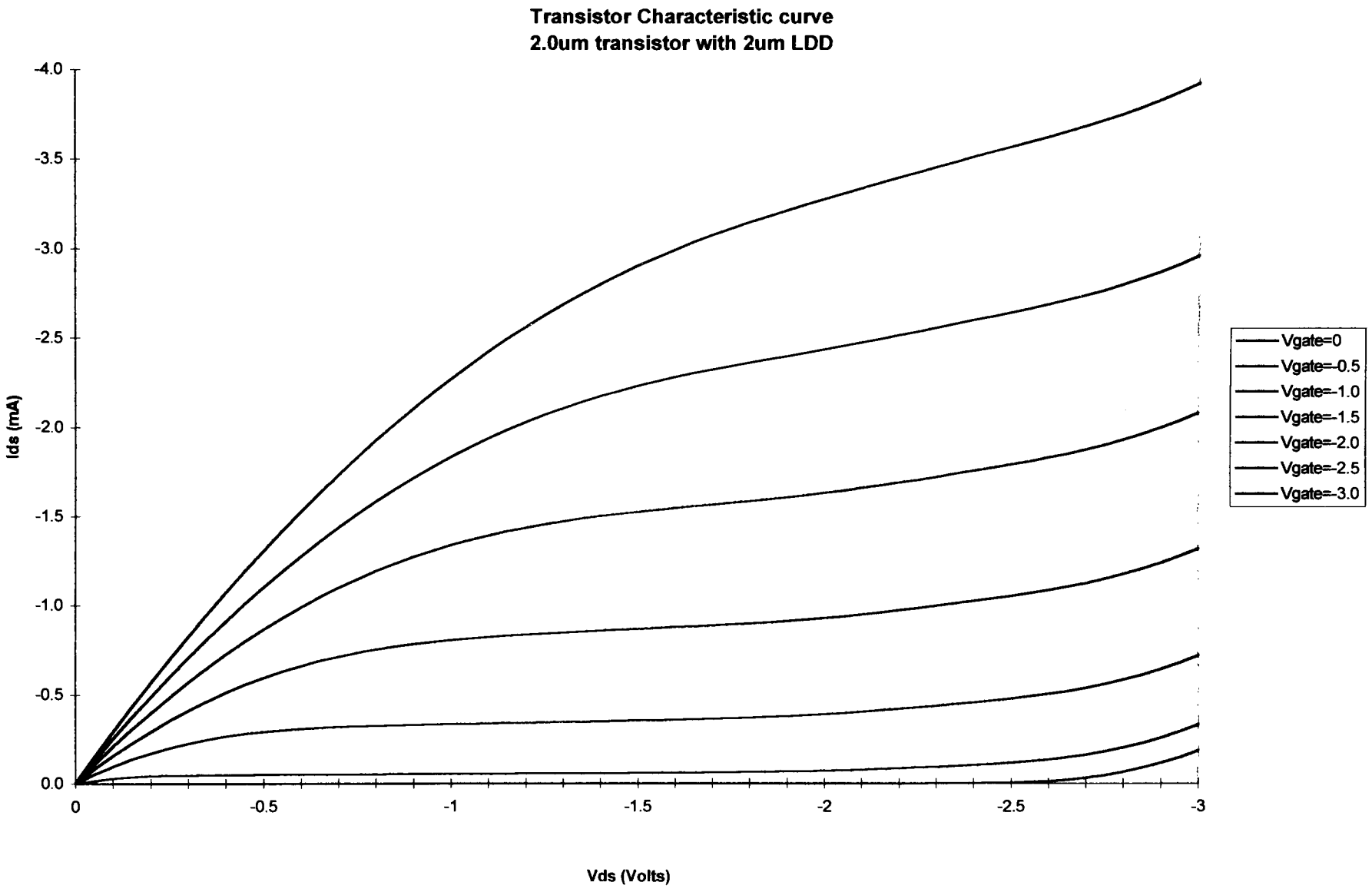

Equipotential surfaces Gate=-4.0v Drain=-5.0v
Distance (Microns)
0.00
1.00
10.0
11.0
12.0
13.0
14.0
15.0
16.0
17.0
Distance (Microns)

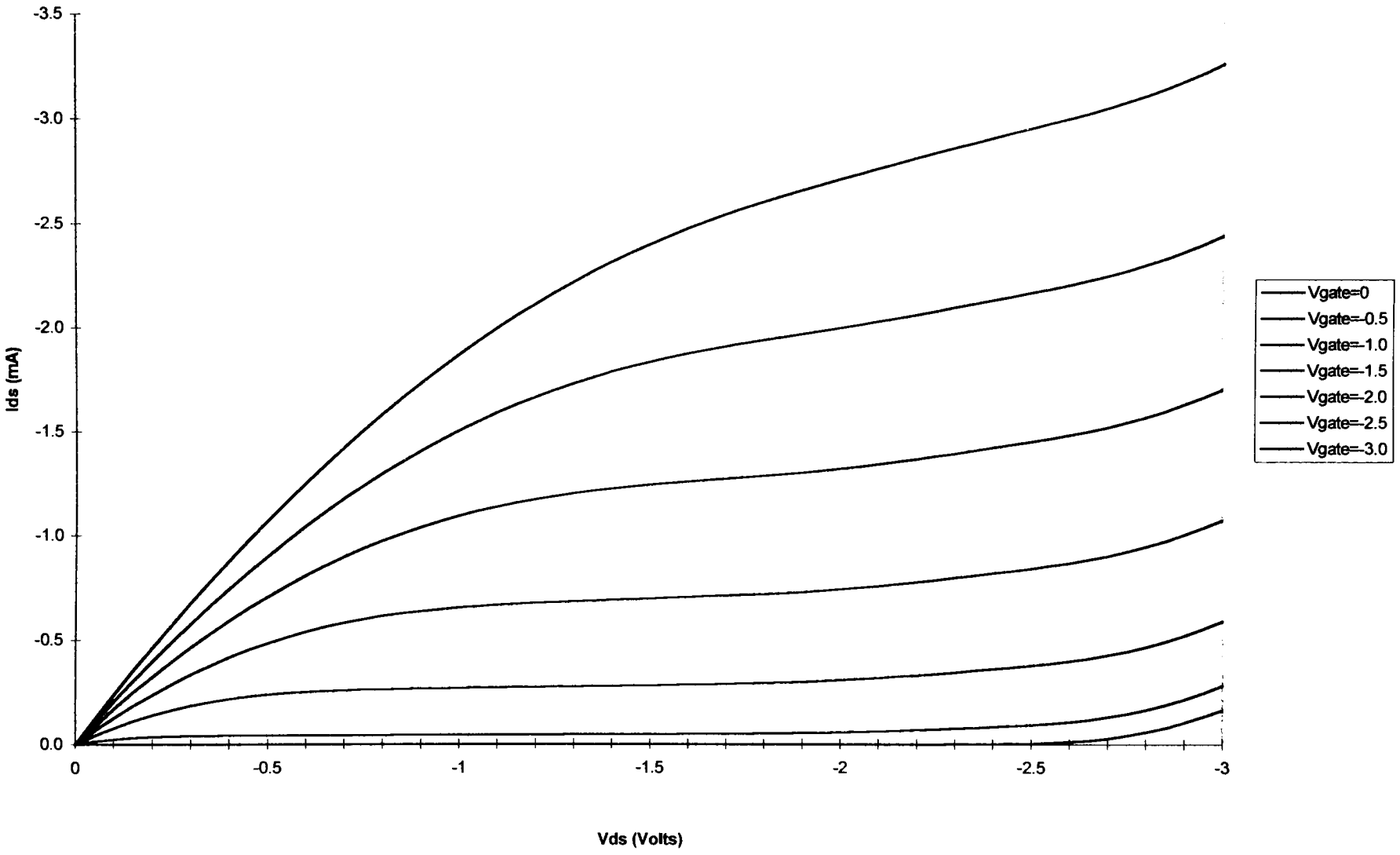

Hole conc. for 5.0 um transistor. Vd=-5 Vg=-4
Distance (Microns)
1.00
500.00
10.0
12.0
14.0
16.0
18.0
Distance (Microns)

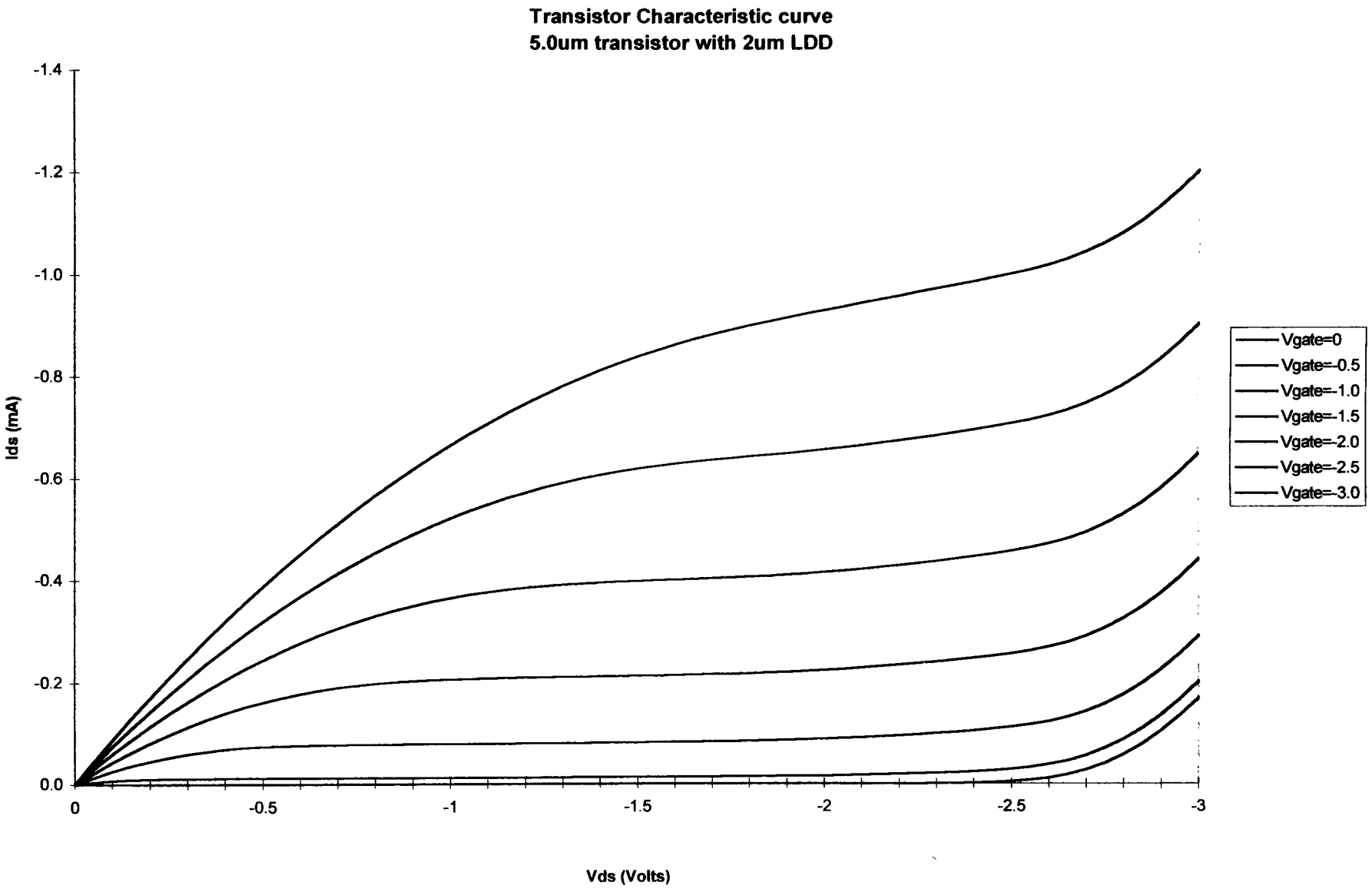
Appendix D - Plots of transistor characteristics

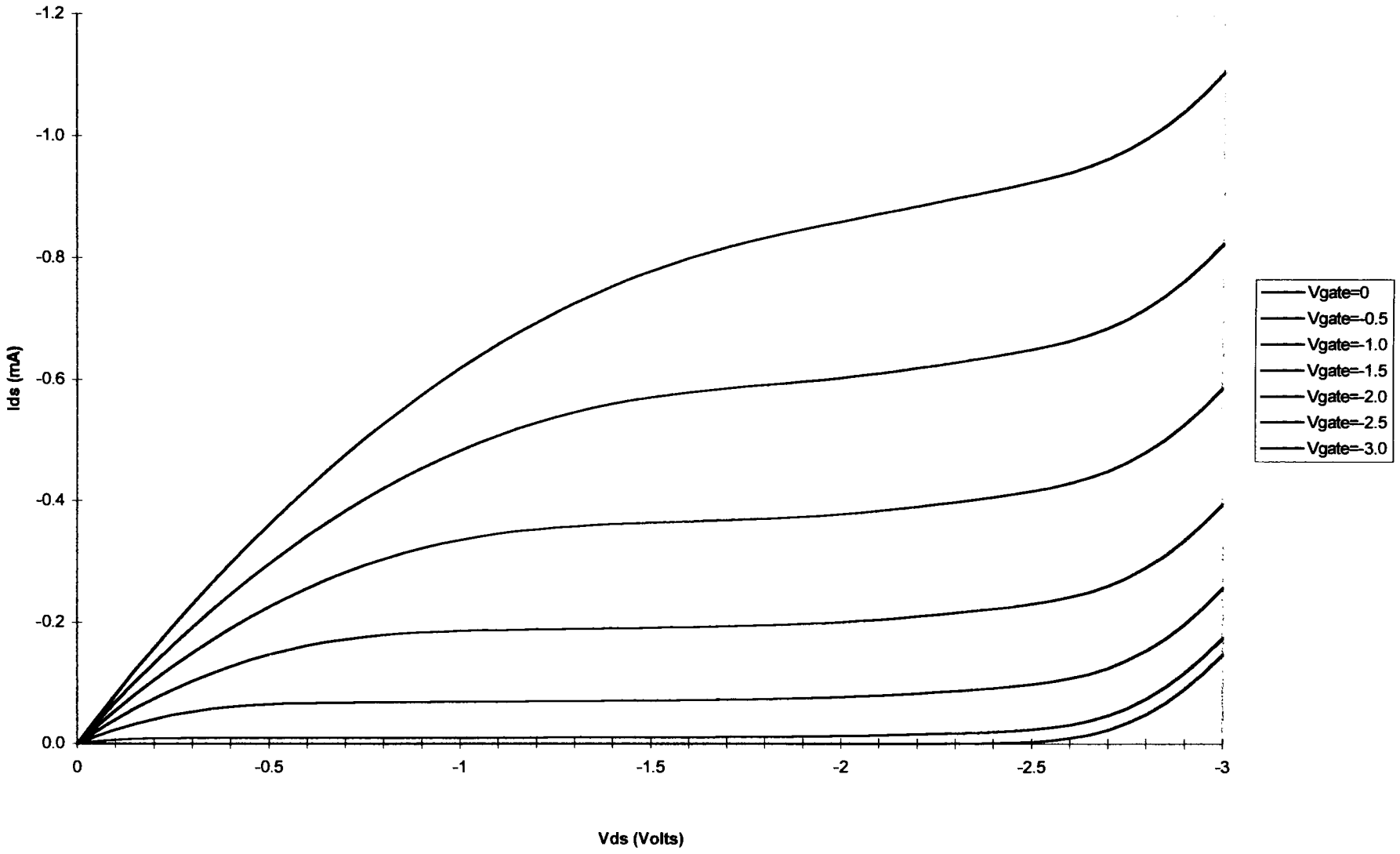

Transistor Characteristic curve
.75um transistor with 2um LDD
-8.0
-7.0
-6.0
-5.0
-4.0
-3.0
-2.0
-1.0
0.0
Ids (mA)
0
-0.5
-1
-1.5
-2
-2.5
-3
Vds (Volts)
Vgate=0
Vgate=-0.5
Vgate=-1.0
Vgate=-1.5
Vgate=-2.0
Vgate=-2.5
Vgate=-3.0

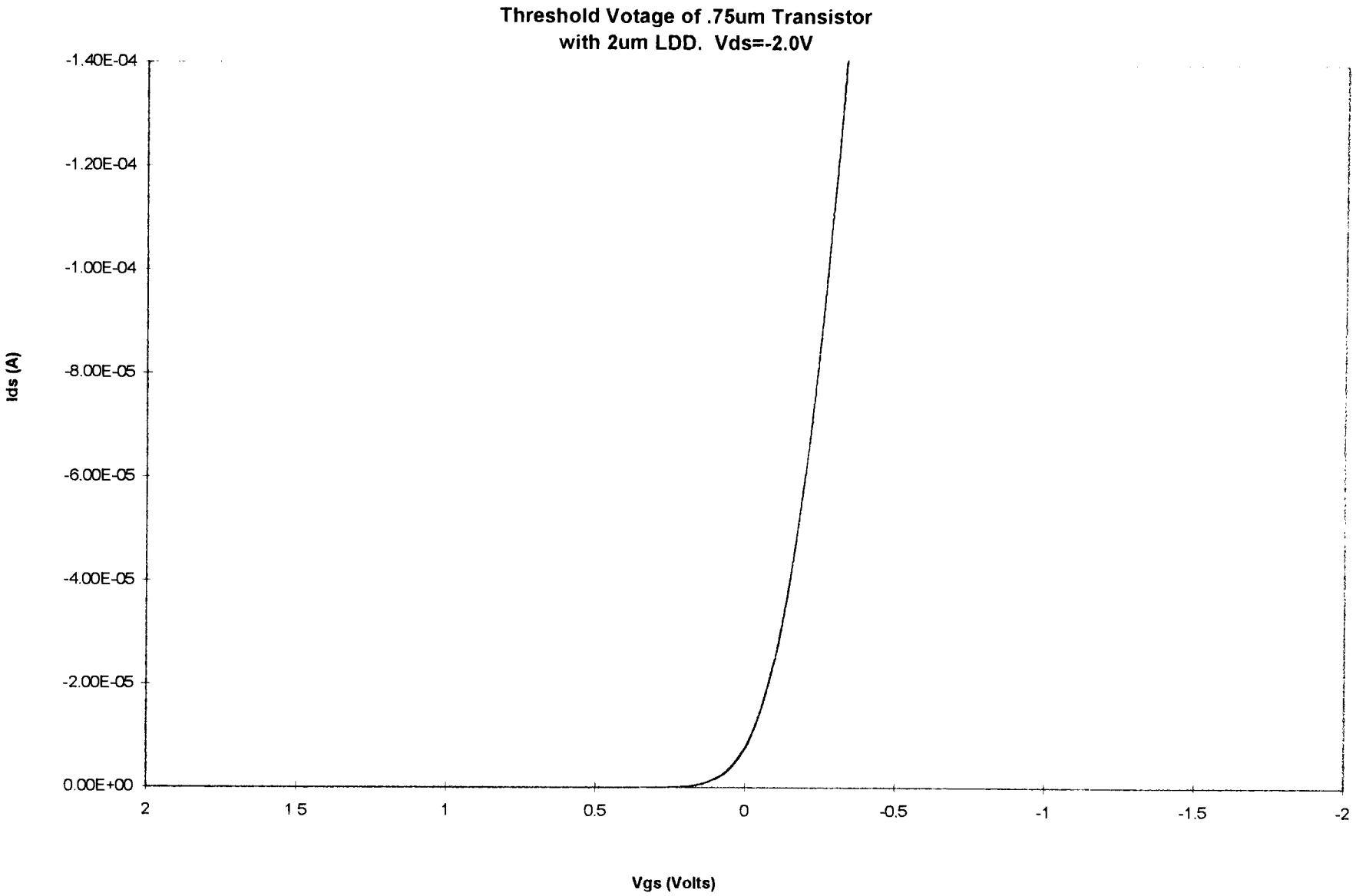

Transistor Characteristic curve
.75um transistor with 5um LDD
-6.0
-5.0
-4.0
-3.0
-2.0
-1.0
0.0
Ids (mA)
0
-0.5
-1
-1.5
-2
-2.5
-3
Vds (Volts)
Vgate=0
Vgate=-0.5
Vgate=-1.0
Vgate=-1.5
Vgate=-2.0
Vgate=-2.5
Vgate=-3.0

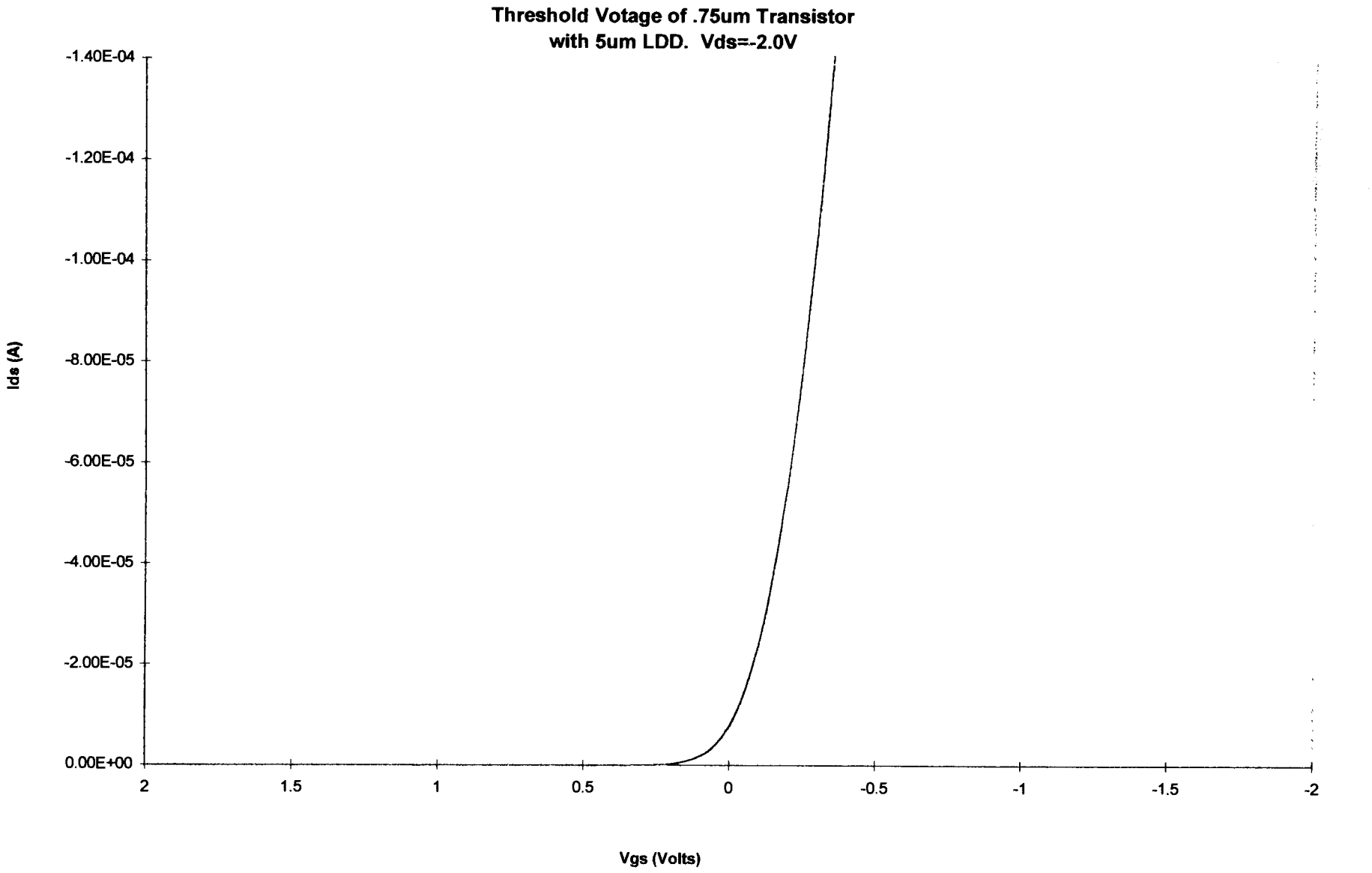

Transistor Characteristic curve
2.0um transistor with 2um LDD
-4.0
-3.5
-3.0
-2.5
-2.0
-1.5
-1.0
-0.5
0.0
Ids (mA)
0
-0.5
-1
-1.5
-2
-2.5
-3
Vds (Volts)
Vgate=0
Vgate=-0.5
Vgate=-1.0
Vgate=-1.5
Vgate=-2.0
Vgate=-2.5
Vgate=-3.0

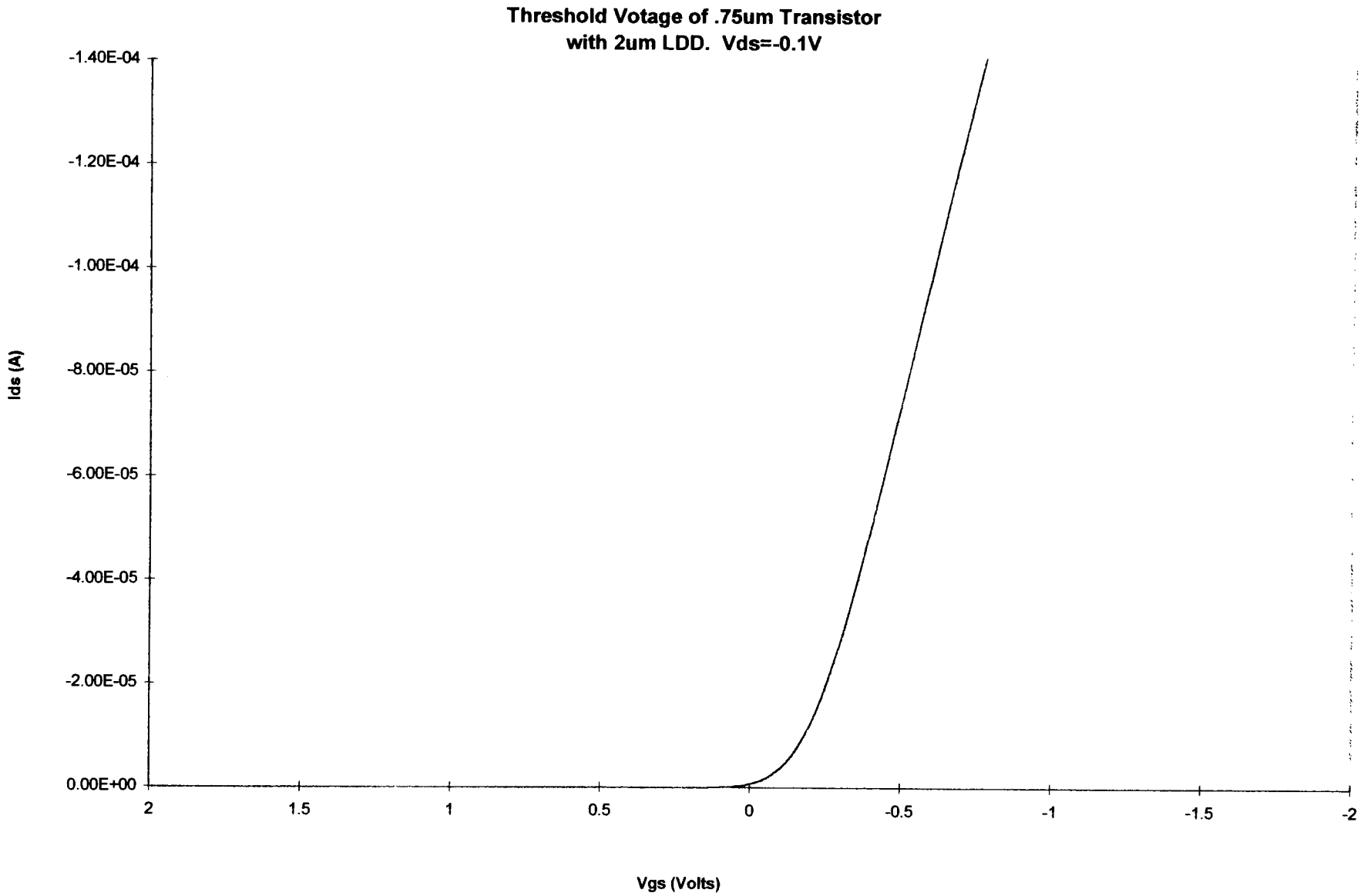

Transistor Characteristic curve
2.0um transistor with 5um LDD
-3.5
-3.0
-2.5
-2.0
-1.5
-1.0
-0.5
0.0
Ids (mA)
0
-0.5
-1
-1.5
-2
-2.5
-3
Vds (Volts)
Vgate=0
Vgate=-0.5
Vgate=-1.0
Vgate=-1.5
Vgate=-2.0
Vgate=-2.5
Vgate=-3.0

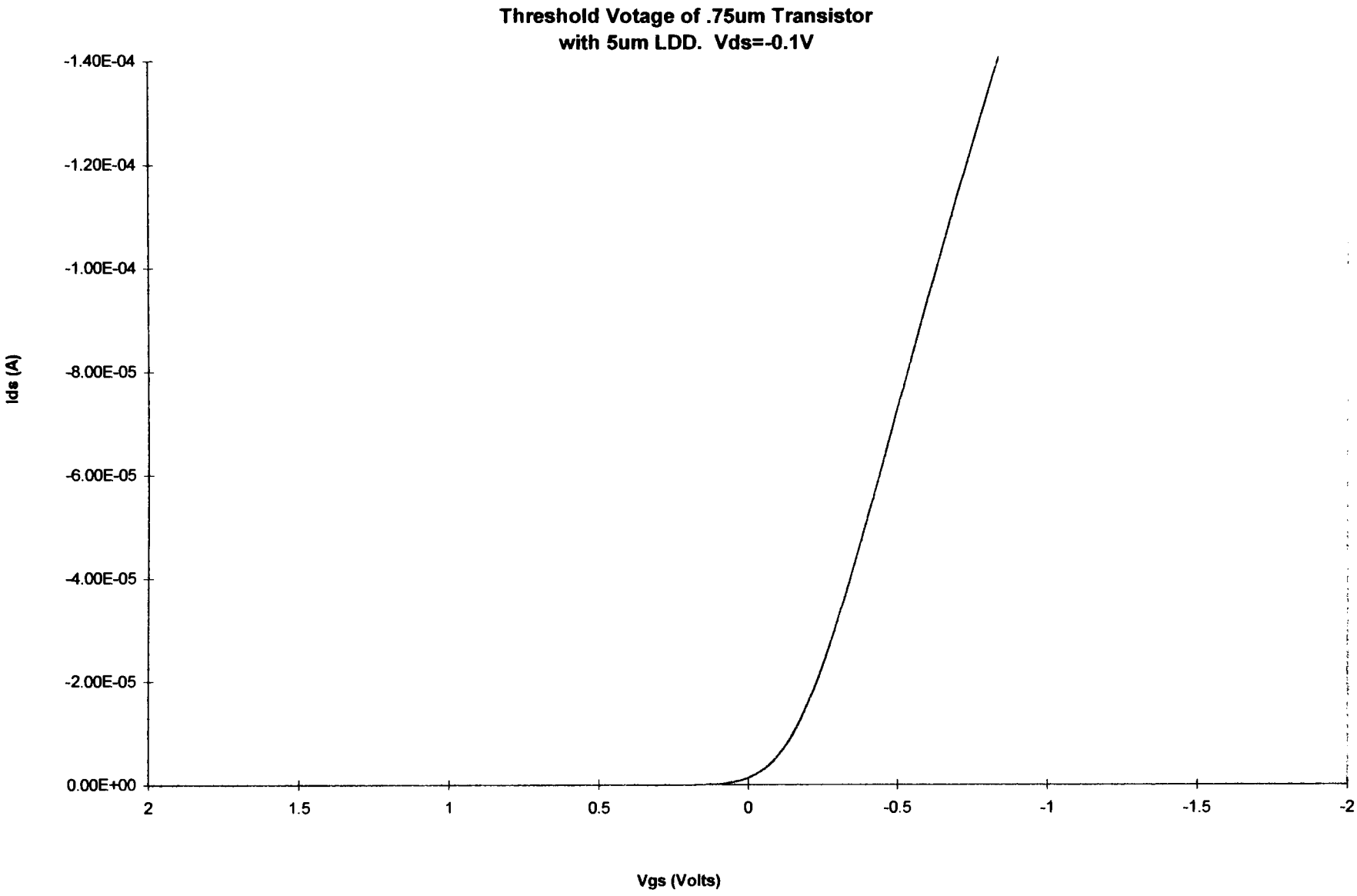

Transistor Characteristic curve
5.0um transistor with 2um LDD
-1.4
-1.2
-1.0
-0.8
-0.6
-0.4
-0.2
0.0
Ids (mA)
0
-0.5
-1
-1.5
-2
-2.5
-3
Vds (Volts)
Vgate=0
Vgate=-0.5
Vgate=-1.0
Vgate=-1.5
Vgate=-2.0
Vgate=-2.5
Vgate=-3.0

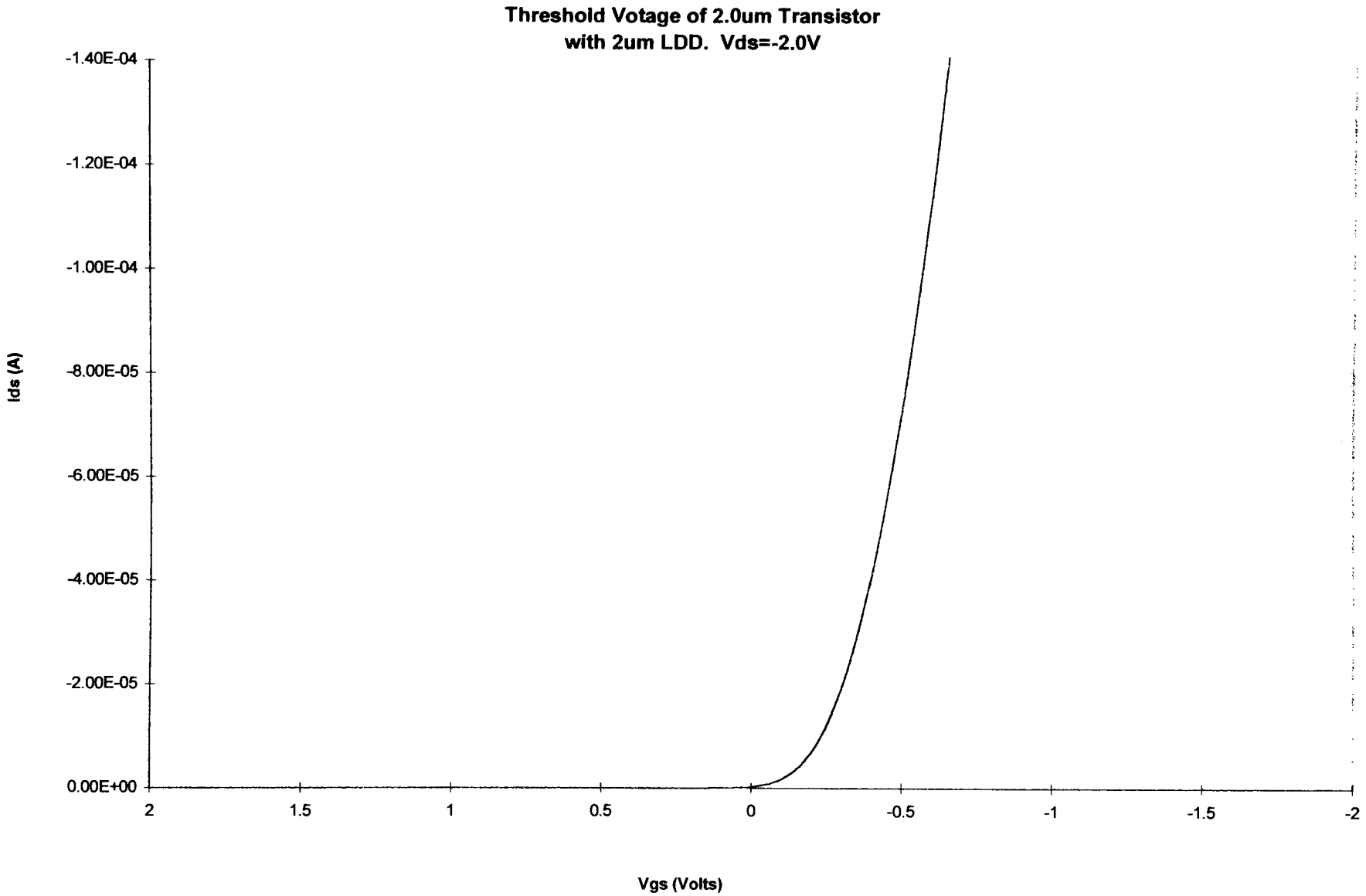

Transistor Characteristic curve
5.0um transistor with 5um LDD
-1.2
-1.0
-0.8
-0.6
-0.4
-0.2
0.0
Ids (mA)
0
-0.5
-1
-1.5
-2
-2.5
-3
Vds (Volts)
Vgate=0
Vgate=-0.5
Vgate=-1.0
Vgate=-1.5
Vgate=-2.0
Vgate=-2.5
Vgate=-3.0

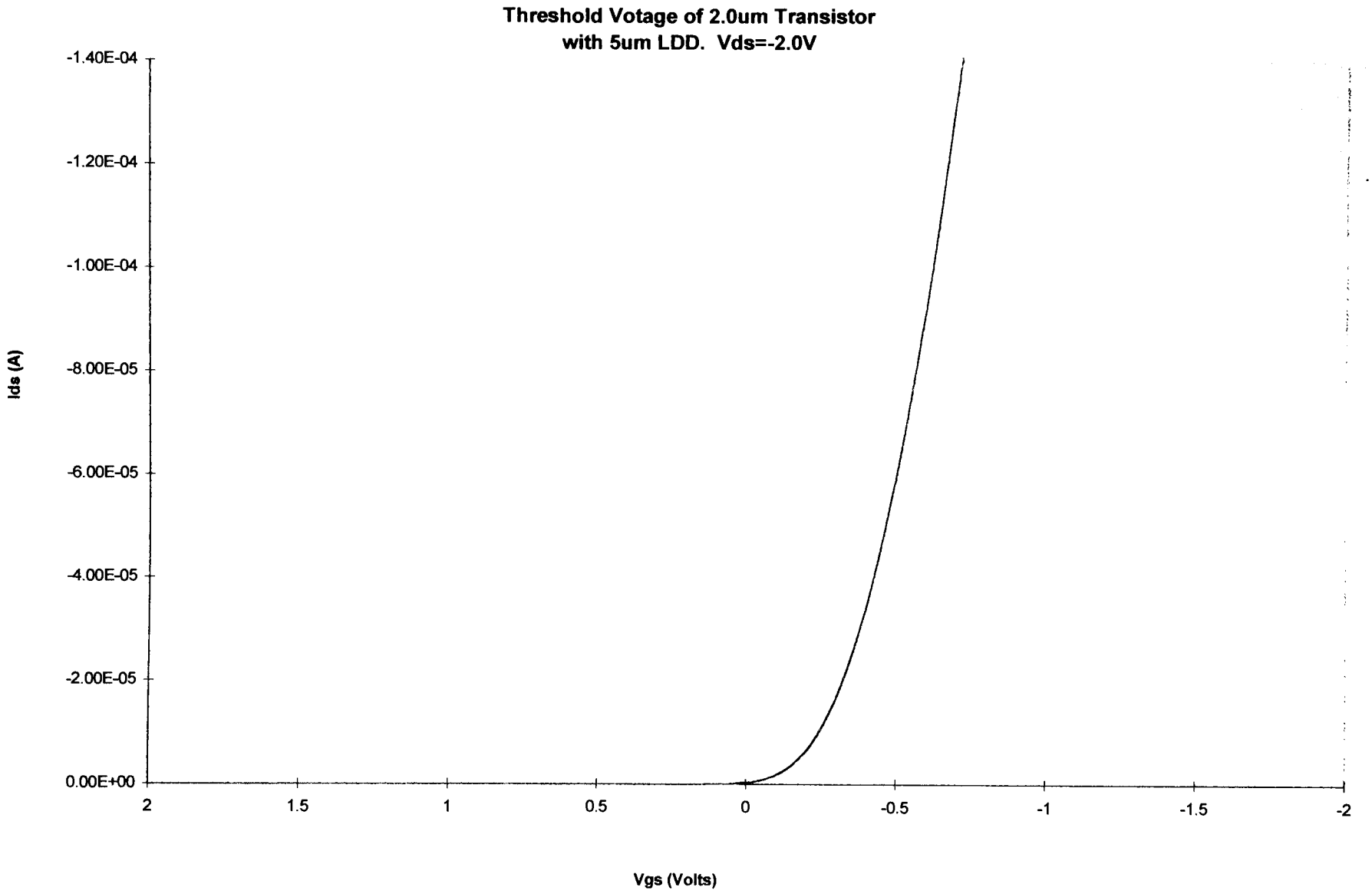

Threshold Votage of .75um Transistor
with 2um LDD. Vds=-2.0V
-1.40E-04
-1.20E-04
-1.00E-04
-8.00E-05
-6.00E-05
-4.00E-05
-2.00E-05
0.00E+00
Ids (A)
2
1 5
1
0.5
0
-0.5
-1
-1.5
-2
Vgs (Volts)

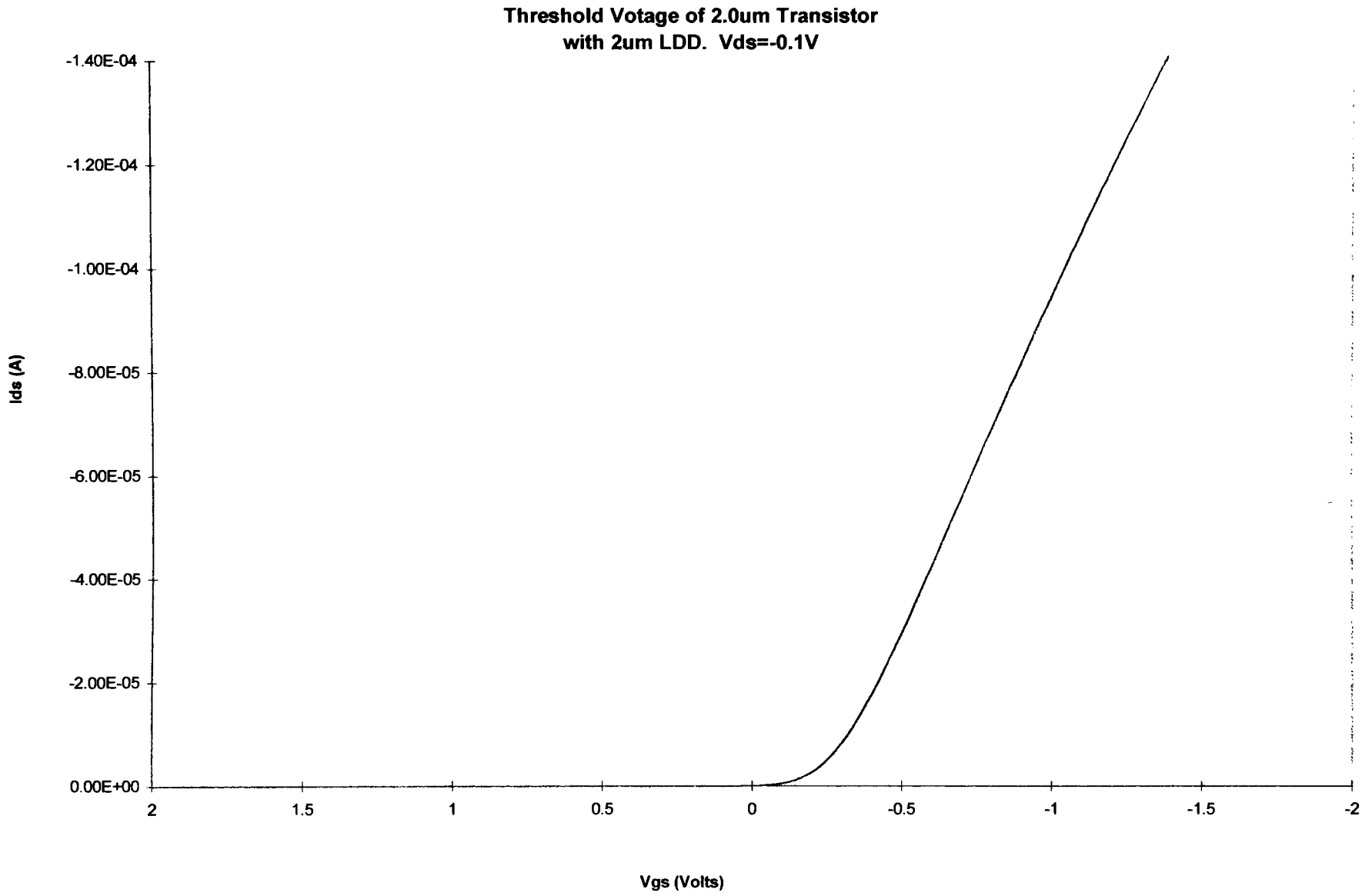

Threshold Votage of .75um Transistor
with 5um LDD. Vds=-2.0V
-1.40E-04
-1.20E-04
-1.00E-04
-8.00E-05
-6.00E-05
-4.00E-05
-2.00E-05
0.00E+00
Ids (A)
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Vgs (Volts)

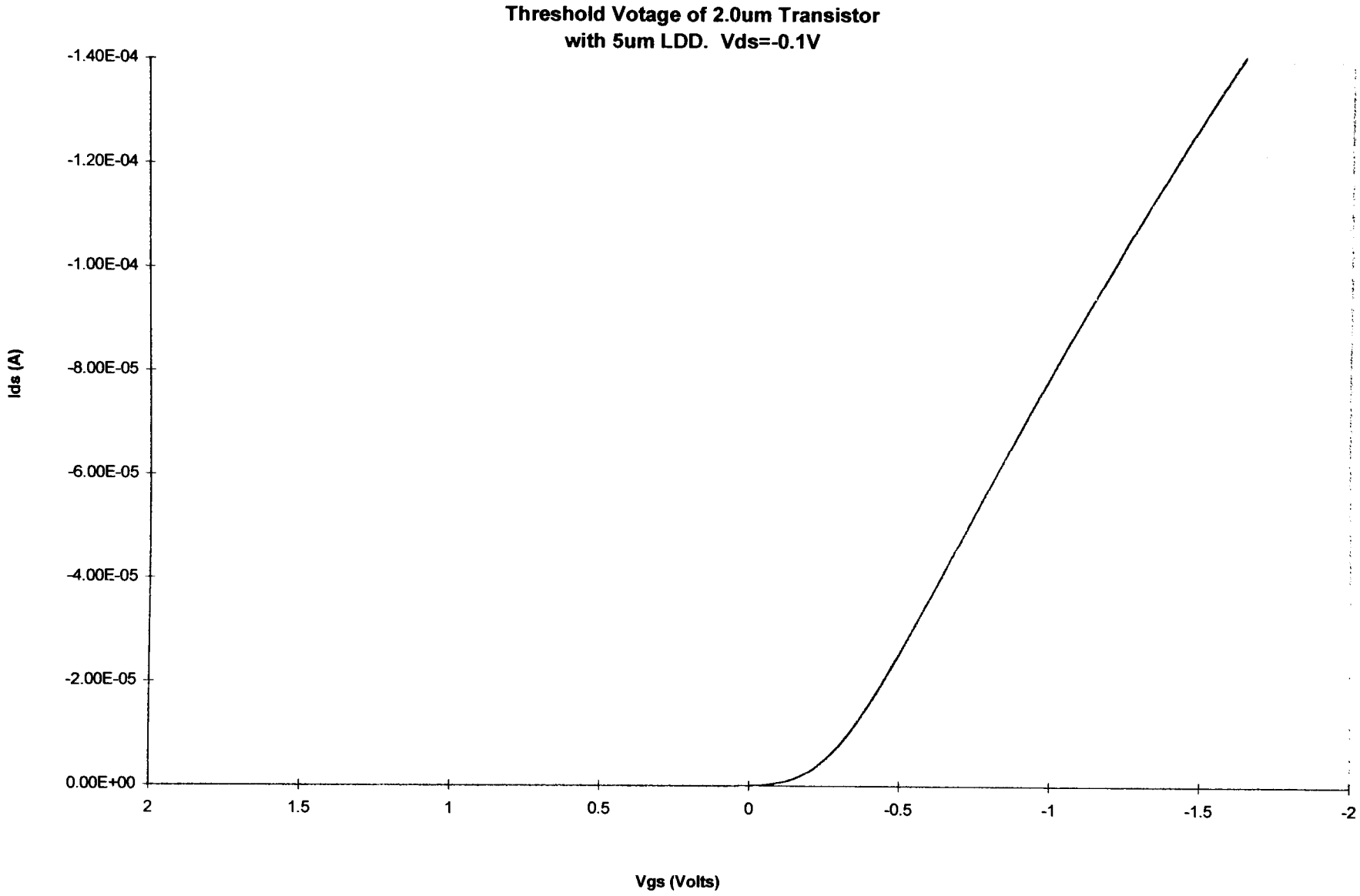

Threshold Votage of .75um Transistor
with 2um LDD. Vds=-0.1V
-1.40E-04
-1.20E-04
-1.00E-04
-8.00E-05
-6.00E-05
-4.00E-05
-2.00E-05
0.00E+00
Ids (A)
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Vgs (Volts)

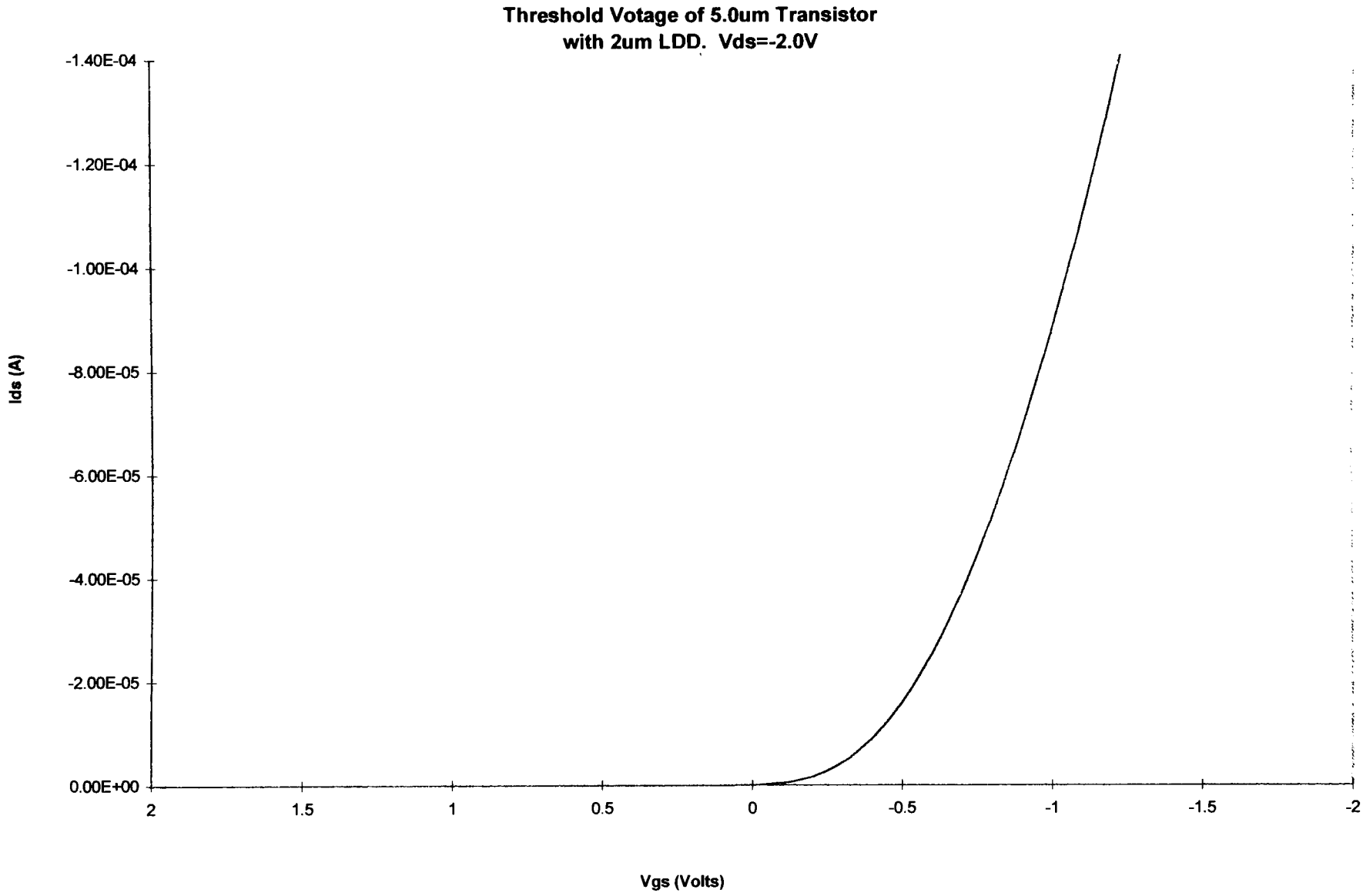

Threshold Votage of .75um Transistor
with 5um LDD. Vds=-0.1V
-1.40E-04
-1.20E-04
-1.00E-04
-8.00E-05
-6.00E-05
-4.00E-05
-2.00E-05
0.00E+00
Ids (A)
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Vgs (Volts)

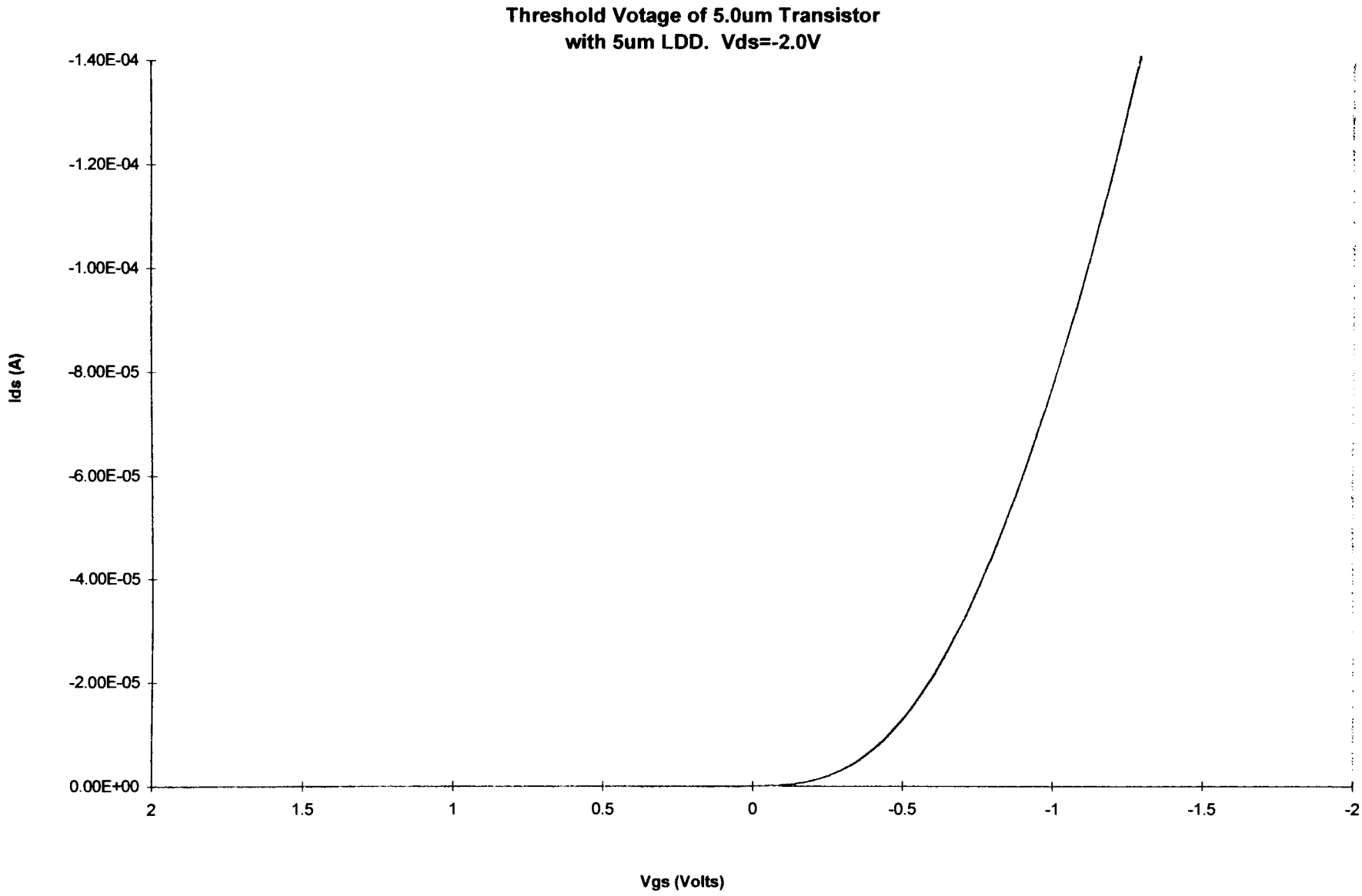

Threshold Votage of 2.0um Transistor
with 2um LDD. Vds=-2.0V
-1.40E-04
-1.20E-04
-1.00E-04
-8.00E-05
-6.00E-05
-4.00E-05
-2.00E-05
0.00E+00
Ids (A)
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Vgs (Volts)

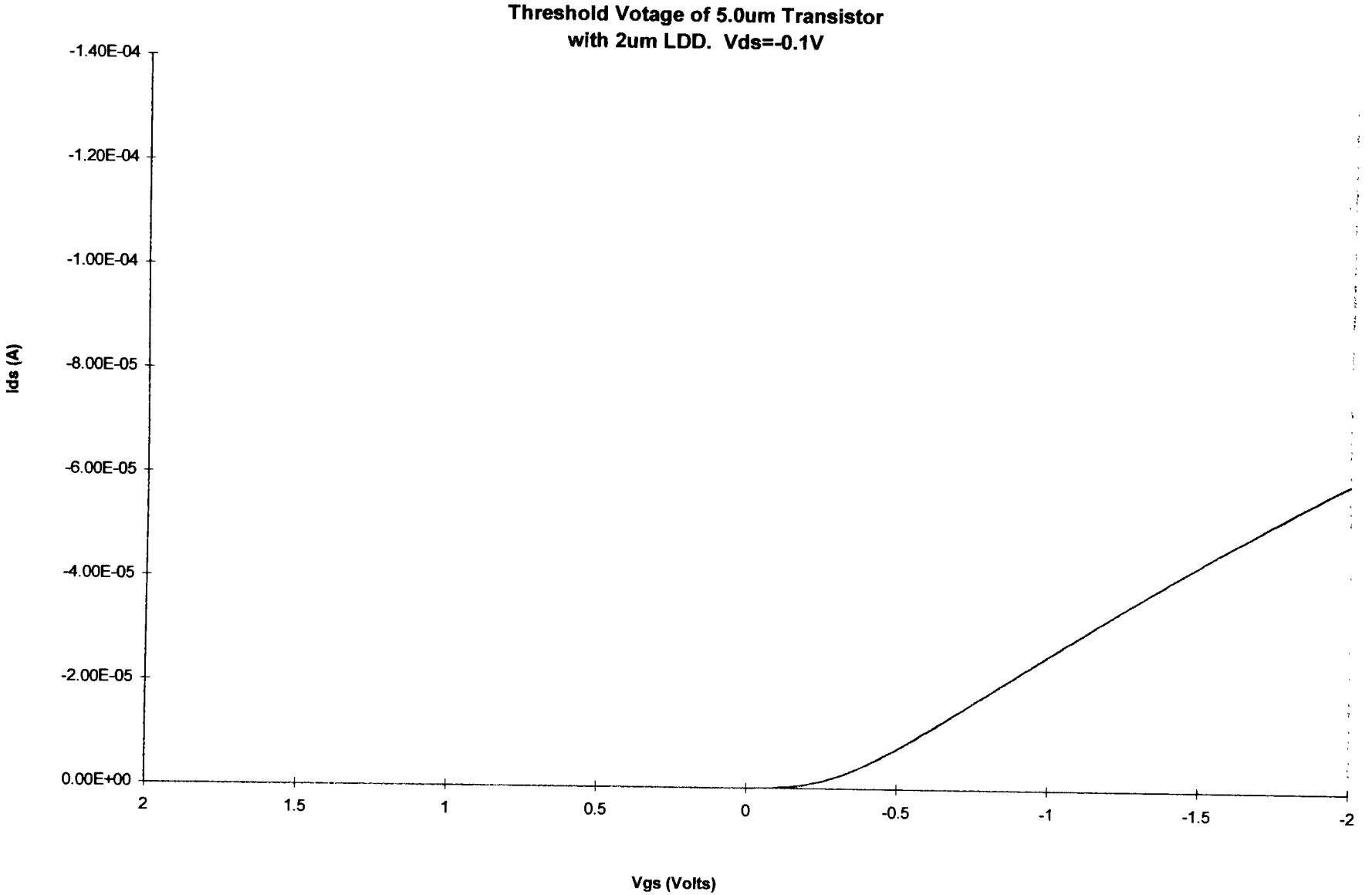

Threshold Votage of 2.0um Transistor
with 5um LDD. Vds=-2.0V
-1.40E-04
-1.20E-04
-1.00E-04
-8.00E-05
-6.00E-05
-4.00E-05
-2.00E-05
0.00E+00
Ids (A)
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Vgs (Volts)

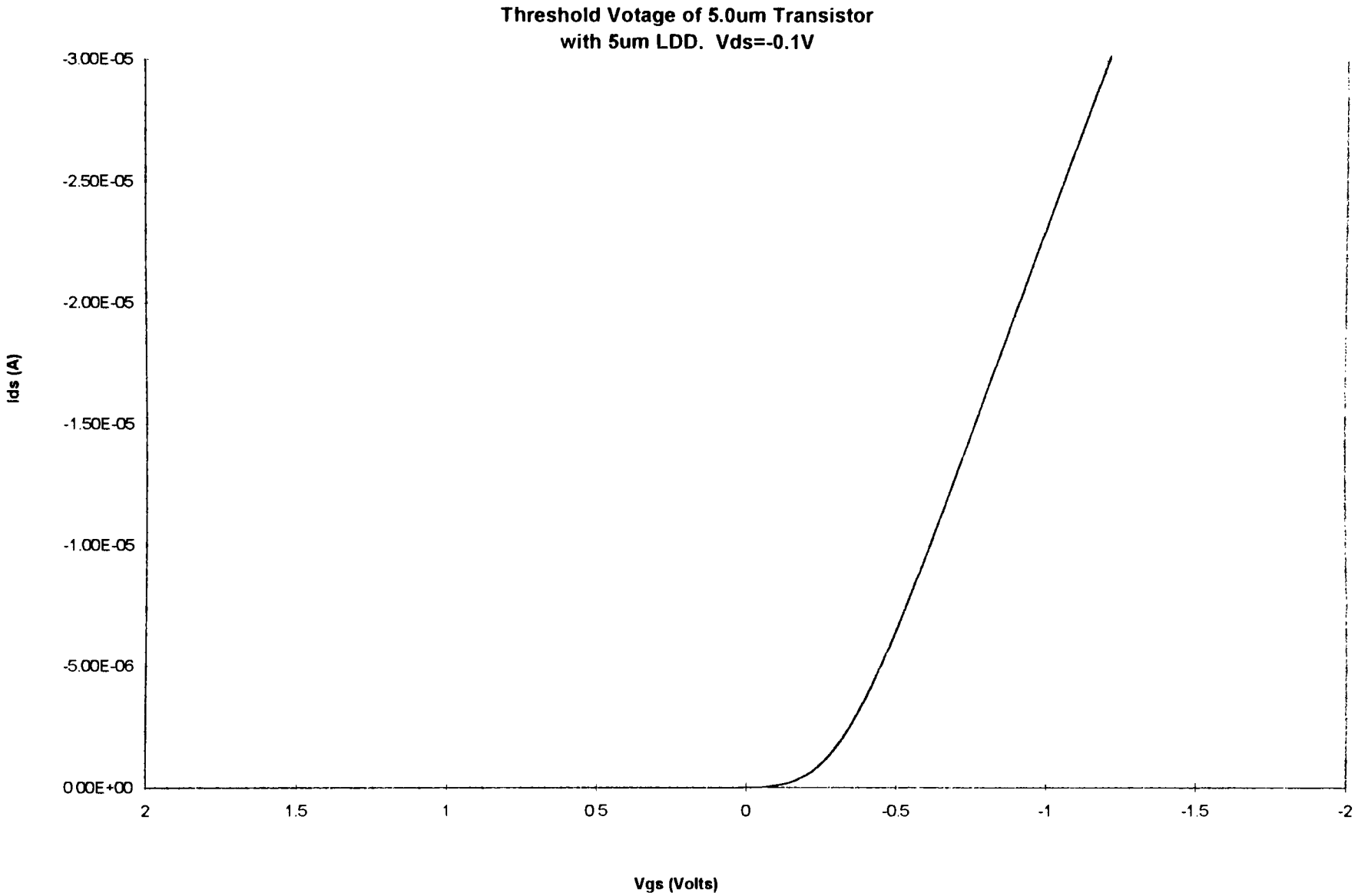

Threshold Votage of 2.0um Transistor
with 2um LDD. Vds=-0.1V
-1.40E-04
-1.20E-04
-1.00E-04
-8.00E-05
-6.00E-05
-4.00E-05
-2.00E-05
0.00E+00
Ids (A)
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Vgs (Volts)

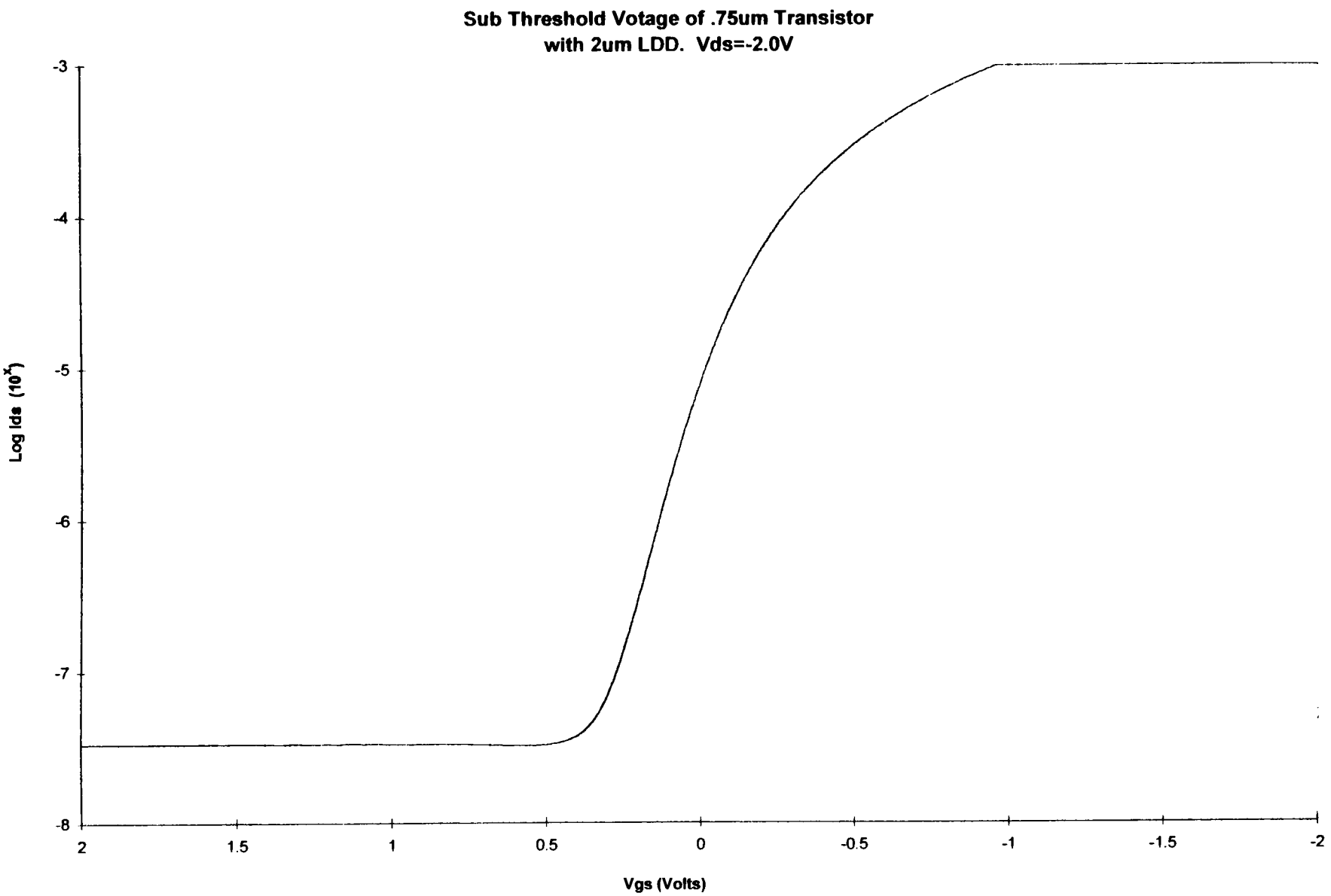

Threshold Votage of 2.0um Transistor
with 5um LDD. Vds=-0.1V
-1.40E-04
-1.20E-04
-1.00E-04
-8.00E-05
-6.00E-05
-4.00E-05
-2.00E-05
0.00E+00
Ids (A)
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Vgs (Volts)

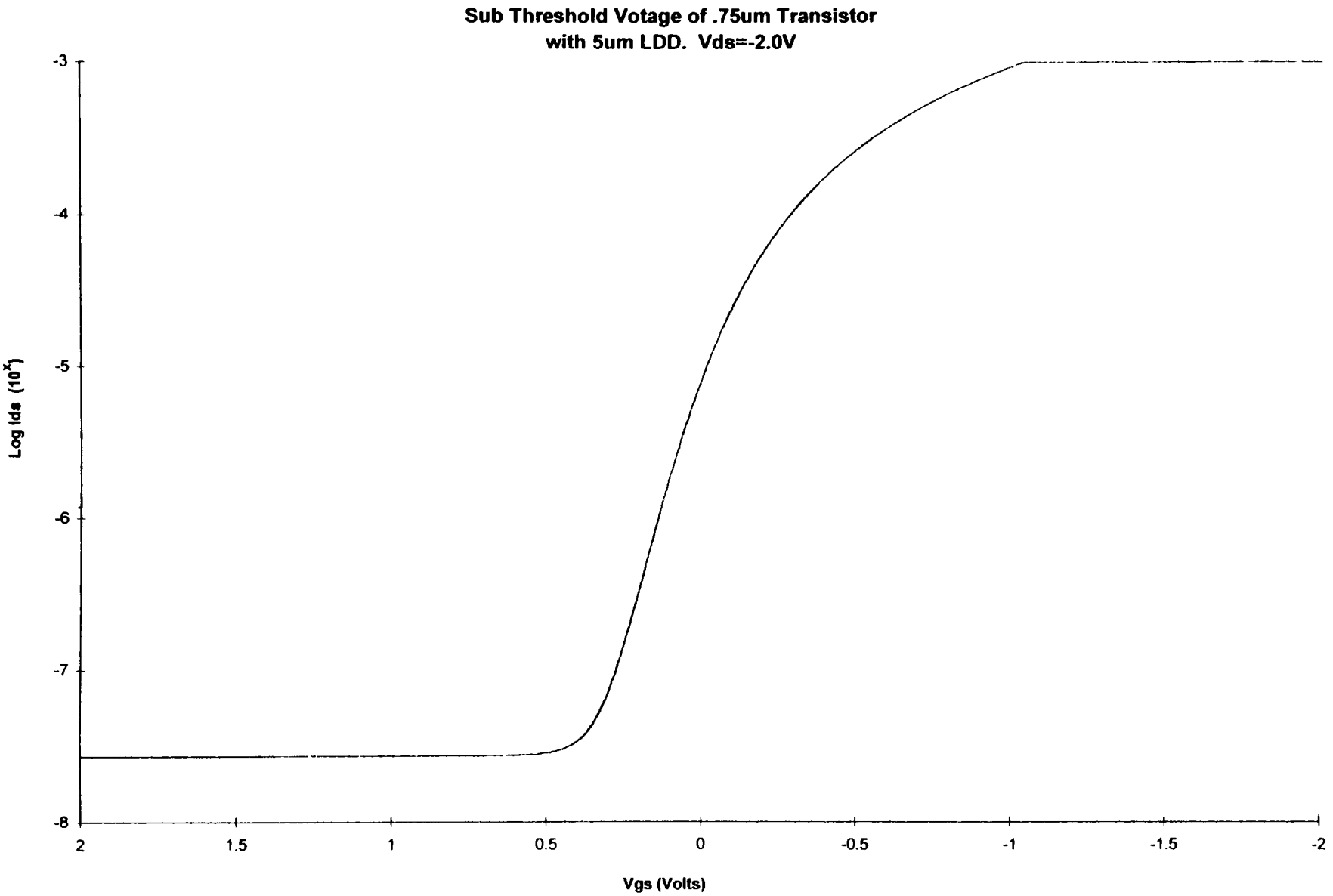

Threshold Votage of 5.0um Transistor
with 2um LDD. Vds=-2.0V
-1.40E-04
-1.20E-04
-1.00E-04
-8.00E-05
-6.00E-05
-4.00E-05
-2.00E-05
0.00E+00
Ids (A)
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Vgs (Volts)

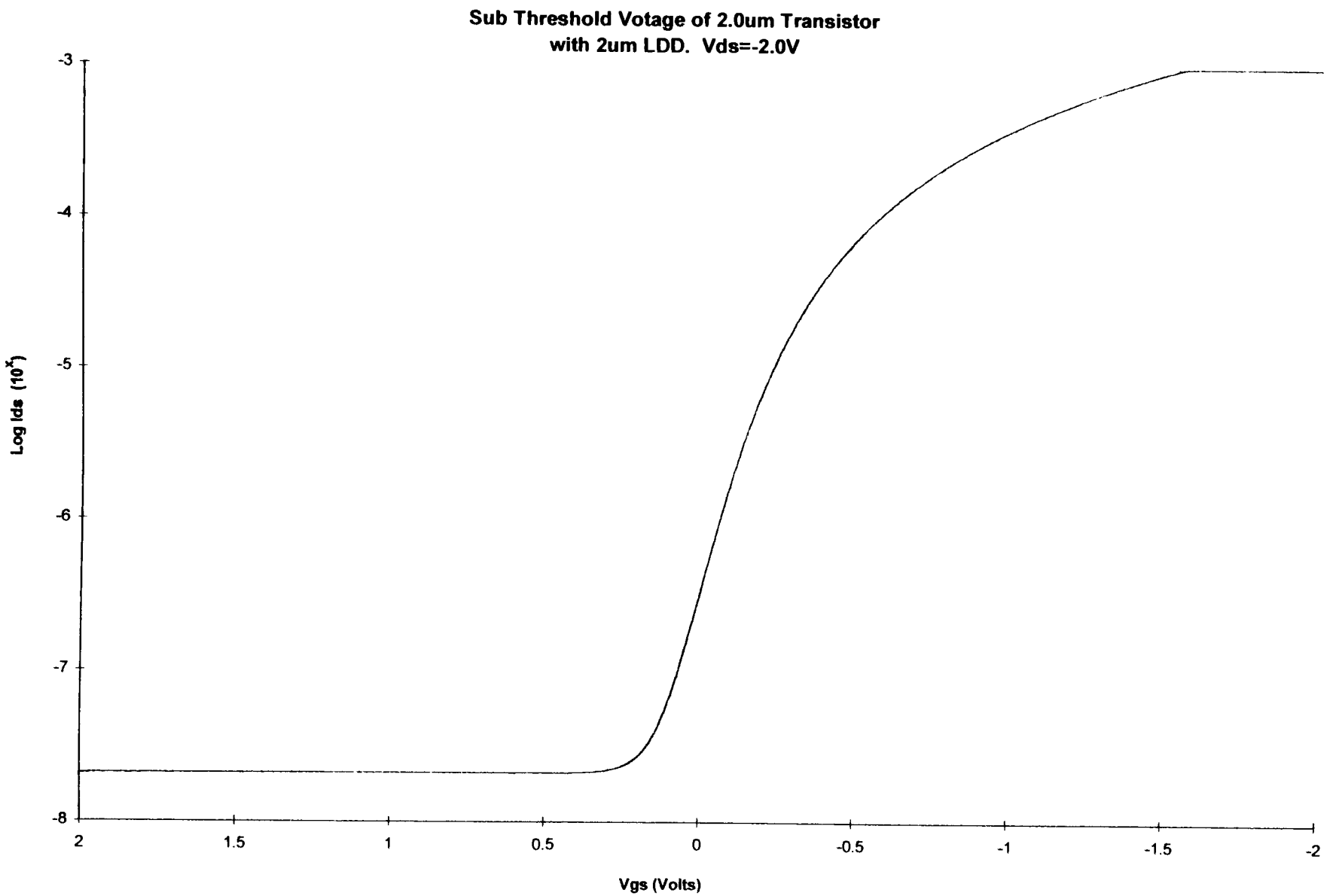

Threshold Votage of 5.0um Transistor
with 5um LDD. Vds=-2.0V
-1.40E-04
-1.20E-04
-1.00E-04
-8.00E-05
-6.00E-05
-4.00E-05
-2.00E-05
0.00E+00
Ids (A)
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Vgs (Volts)

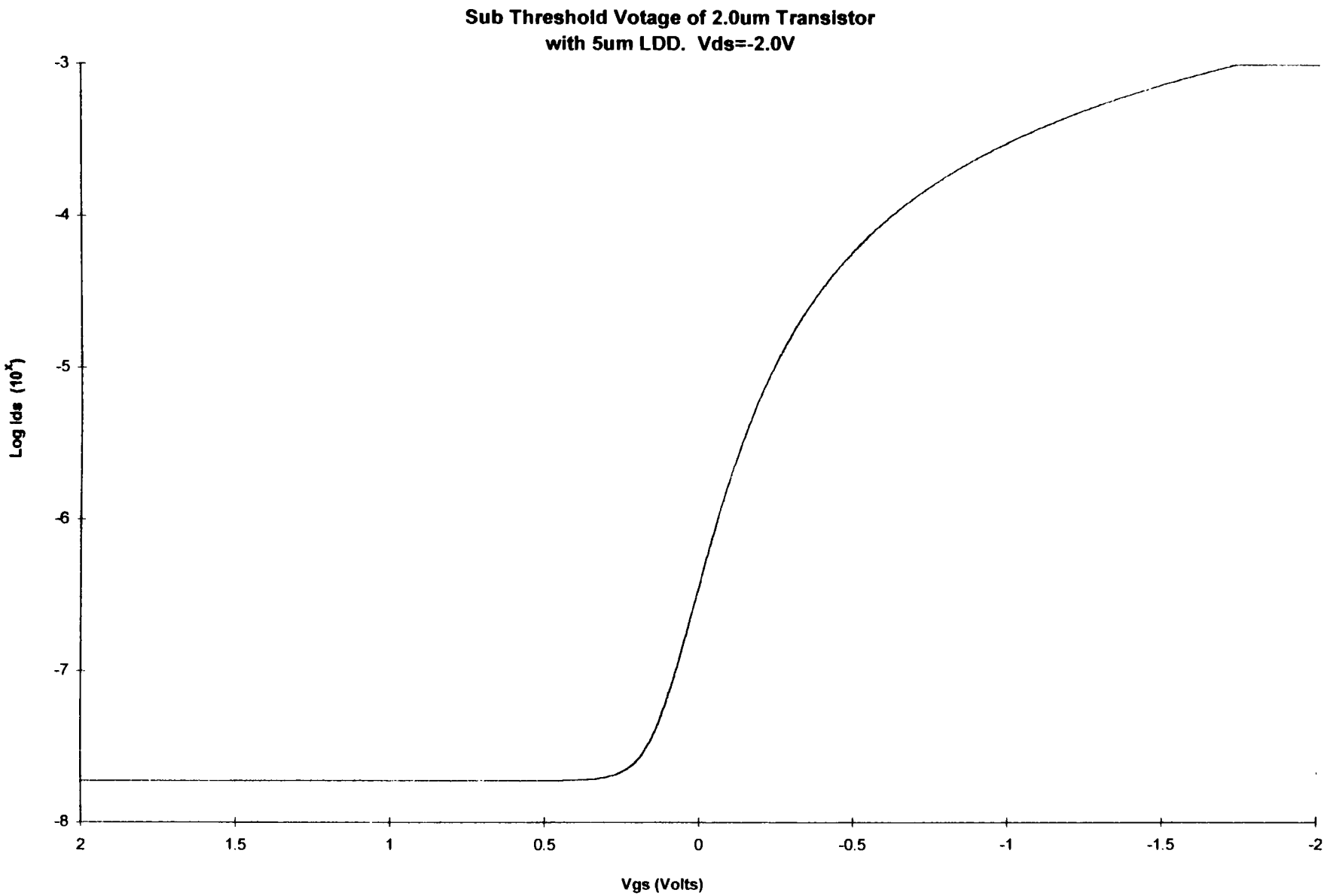

Threshold Votage of 5.0um Transistor
with 2um LDD. Vds=-0.1V
-1.40E-04
-1.20E-04
-1.00E-04
-8.00E-05
-6.00E-05
-4.00E-05
-2.00E-05
0.00E+00
Ids (A)
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Vgs (Volts)

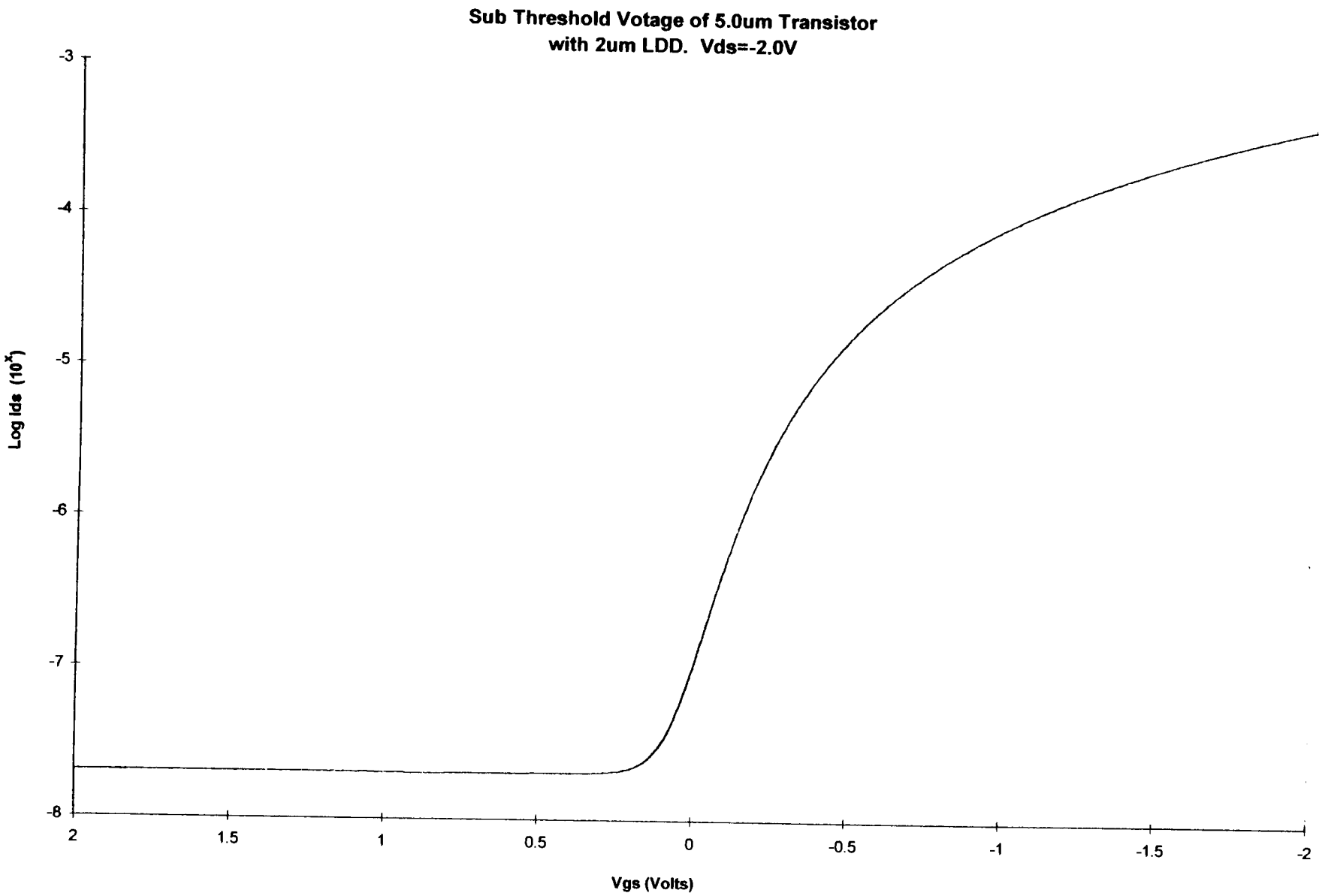

Threshold Votage of 5.0um Transistor
with 5um LDD. Vds=-0.1V
-3.00E-05
-2.50E-05
-2.00E-05
-1.50E-05
-1.00E-05
-5.00E-06
0.00E+00
Ids (A)
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Vgs (Volts)

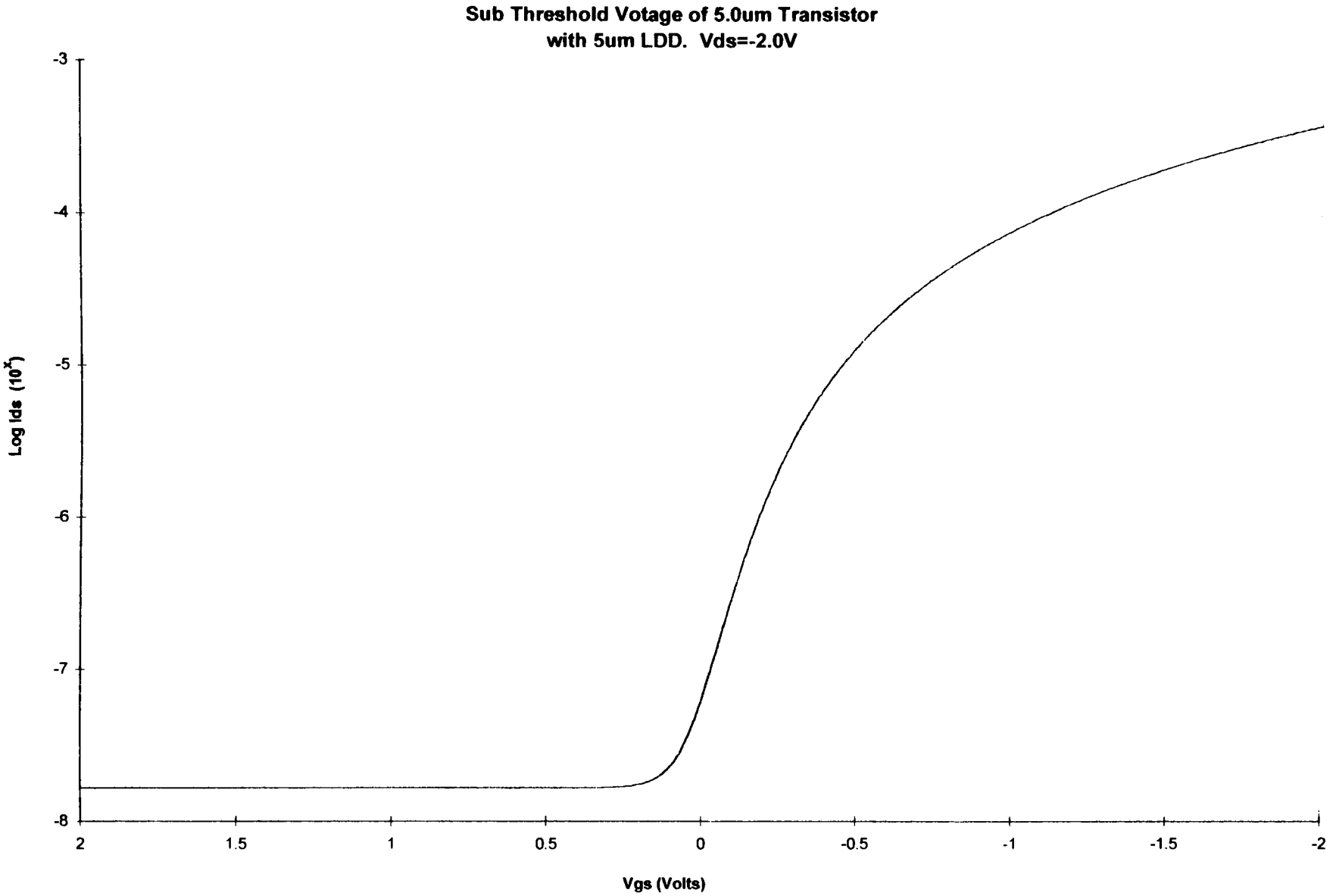

Sub Threshold Votage of .75um Transistor
with 2um LDD. Vds=-2.0V
Log Ids (10^X)
-3
-4
-5
-6
-7
-8
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Vgs (Volts)


Sub Threshold Votage of .75um Transistor
with 5um LDD. Vds=-2.0V
Log Ids (10^X)
-3
-4
-5
-6
-7
-8
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Vgs (Volts)


Sub Threshold Votage of 2.0um Transistor
with 2um LDD. Vds=-2.0V
-3
-4
-5
-6
-7
-8
Log Ids (10^x)
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Vgs (Volts)


Sub Threshold Votage of 2.0um Transistor
with 5um LDD. Vds=-2.0V
Log Ids (10^x)
-3
-4
-5
-6
-7
-8
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Vgs (Volts)


Sub Threshold Votage of 5.0um Transistor
with 2um LDD. Vds=-2.0V
Log Ids (10^X)
-3
-4
-5
-6
-7
-8
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Vgs (Volts)


Sub Threshold Votage of 5.0um Transistor
with 5um LDD. Vds=-2.0V
Log Ids (10^X)
-3
-4
-5
-6
-7
-8
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
Vgs (Volts)

Bibliography

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6. Yanis P. Tsividis, Operation and modeling of the MOS Transistor, McGraw-Hill, New York.